

Bolt Schematic

Whiskey Lake

2018/12/13
REV: A00

DY : None Installed

UMA: UMA only installed

OPS: DISCRTE OPTIMUS installed

TypeC: CCG4

TypeC_5V_OUT: provide external device power 5V

TypeC_PWR_IN: Provide system power via typeC connector.

8111H:Reltek LAN RTL811H

81106E:Reltek LAN RTL8106E

BOLT L 0823

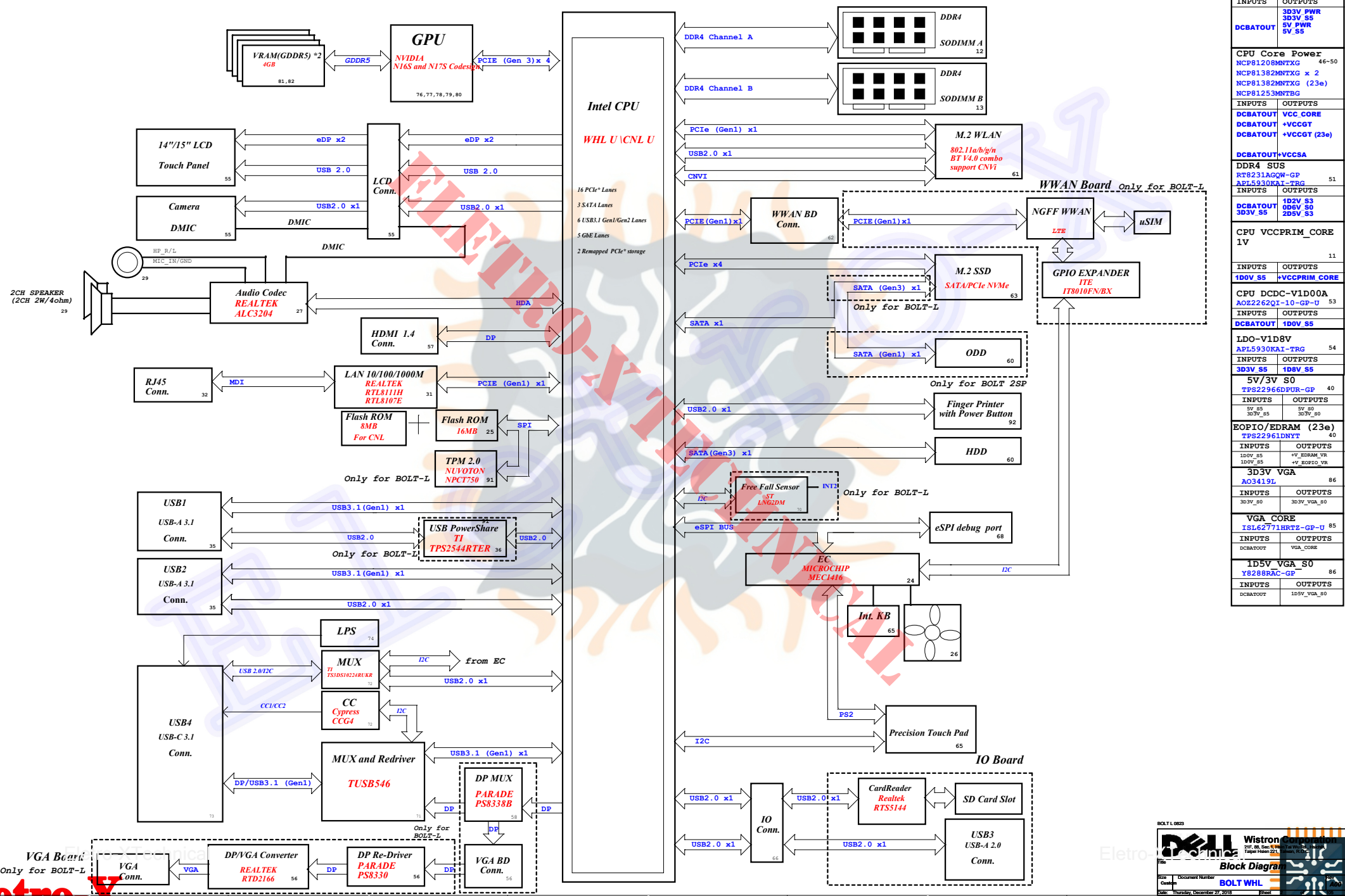
DELL Wistron Corporation
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Title: **Cover Page**
Size: A3 Document Number: **BOLT WHL**
Date: Thursday, December 27, 2018 Sheet 1 of 1



Project Code : 4PD0G7010001
PCB P/N : 18763
Revision : SD

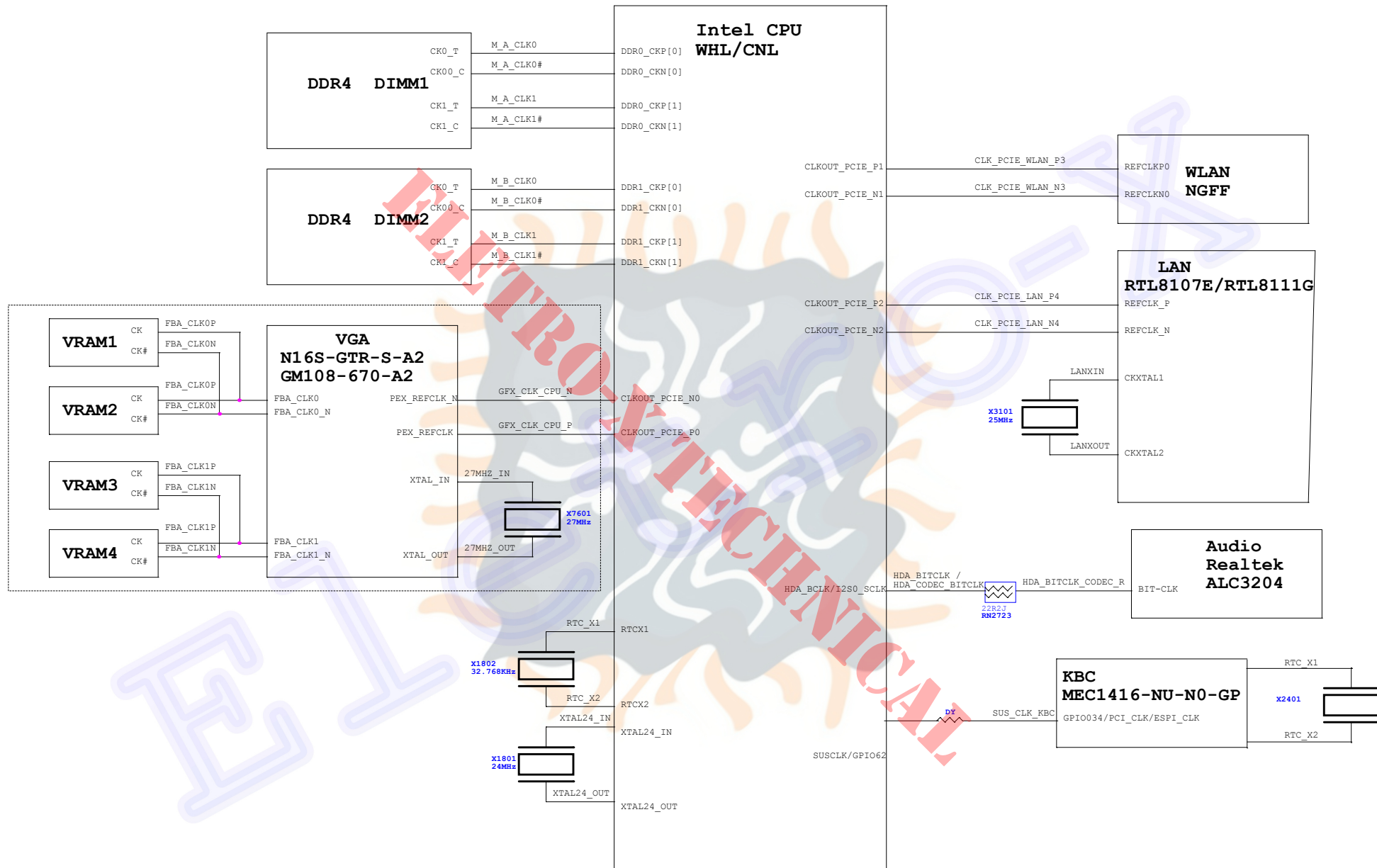
Bolt WHL Block Diagram



CHARGER	
ISL88739	44
INPUTS	
AD+	DCBATOUT
SYSTEM DC/DC	
TPS51225RUKR-GP	45
INPUTS	
DCBATOUT	303V PWR 303V SS 5V PWR 5V SS
CPU Core Power	
NCP81208MNTXG	46-50
NCP81382MNTXG x 2	
NCP81382MNTXG (23e)	
NCP81253MNTBG	
INPUTS	
DCBATOUT	VCC CORE
DCBATOUT	+VCCGT
DCBATOUT	+VCCGT (23e)
DCBATOUT+VCCSA	
DDR4 SUS	
RT8231AGW-GP	51
APL5930KAI-TRG	
INPUTS	
DCBATOUT	102V S3 303V S3 205V S3
CPU VCCPRIM_CORE	
1V	11
INPUTS	
100V SS	+VCCPRIM CORE
CPU DCDC-V1D00A	
AO22262QI-10-GP-U	53
INPUTS	
DCBATOUT	100V SS
LDO-V1D8V	
APL5930KAI-TRG	54
INPUTS	
303V SS	108V SS
5V/3V S0	
TPS22966DPR-GP	40
INPUTS	
5V SS 303V SS	5V SS 303V SS
EOP10/EDRAM (23e)	
TPS22961DNYT	40
INPUTS	
100V SS 100V SS	+V EDRAM VR +V EOP10 VR
3D3V VGA	
AO3419L	86
INPUTS	
303V SS	303V VGA SS
VGA CORE	
ISL62771HRTZ-GP-U	85
INPUTS	
DCBATOUT	VGA CORE
155V VGA S0	
Y8288RAC-GP	86
INPUTS	
DCBATOUT	155V VGA SS

CLK Block Diagram

Eletro-XTechnical



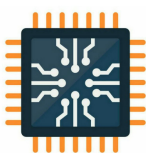
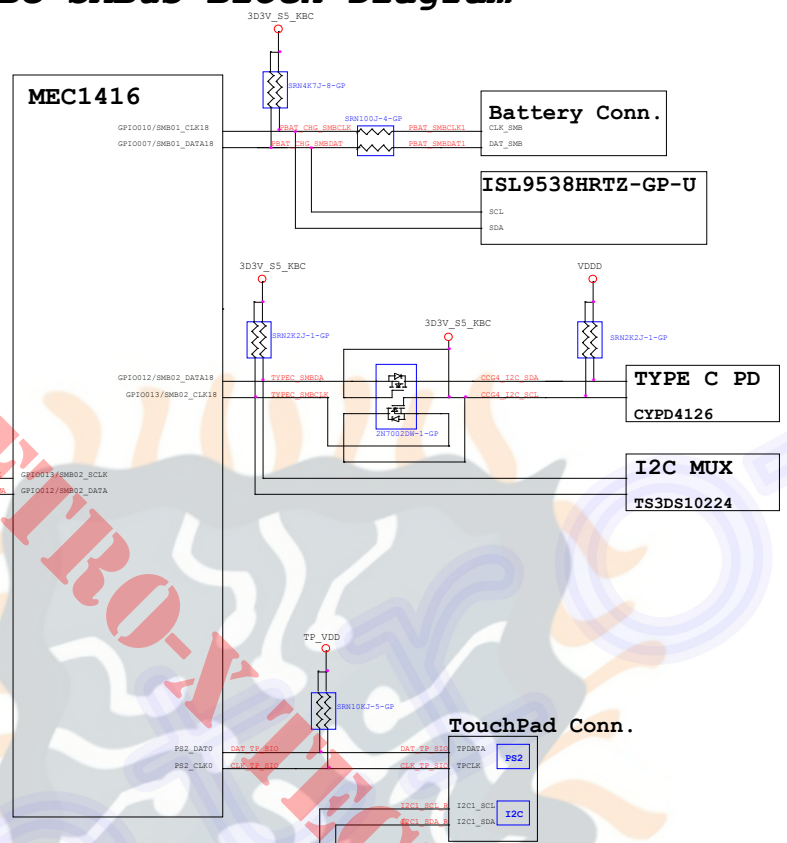
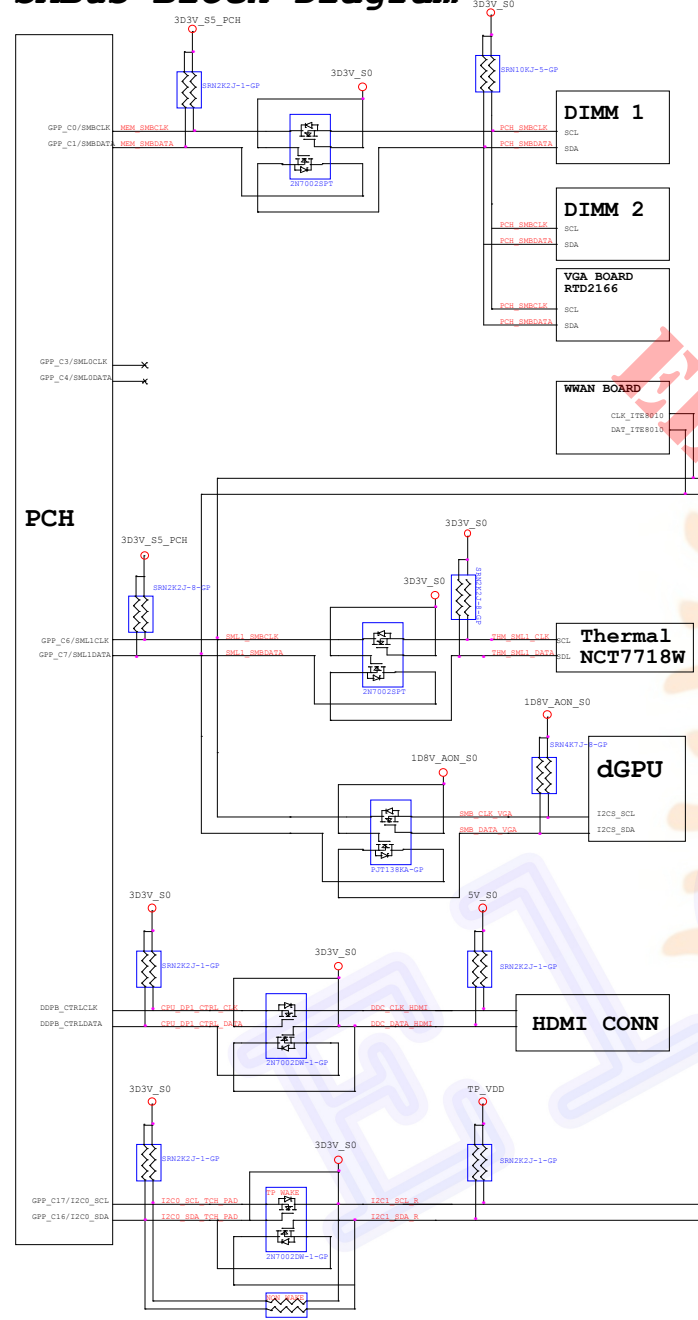
Eletro-XTechnical

Eletro-X

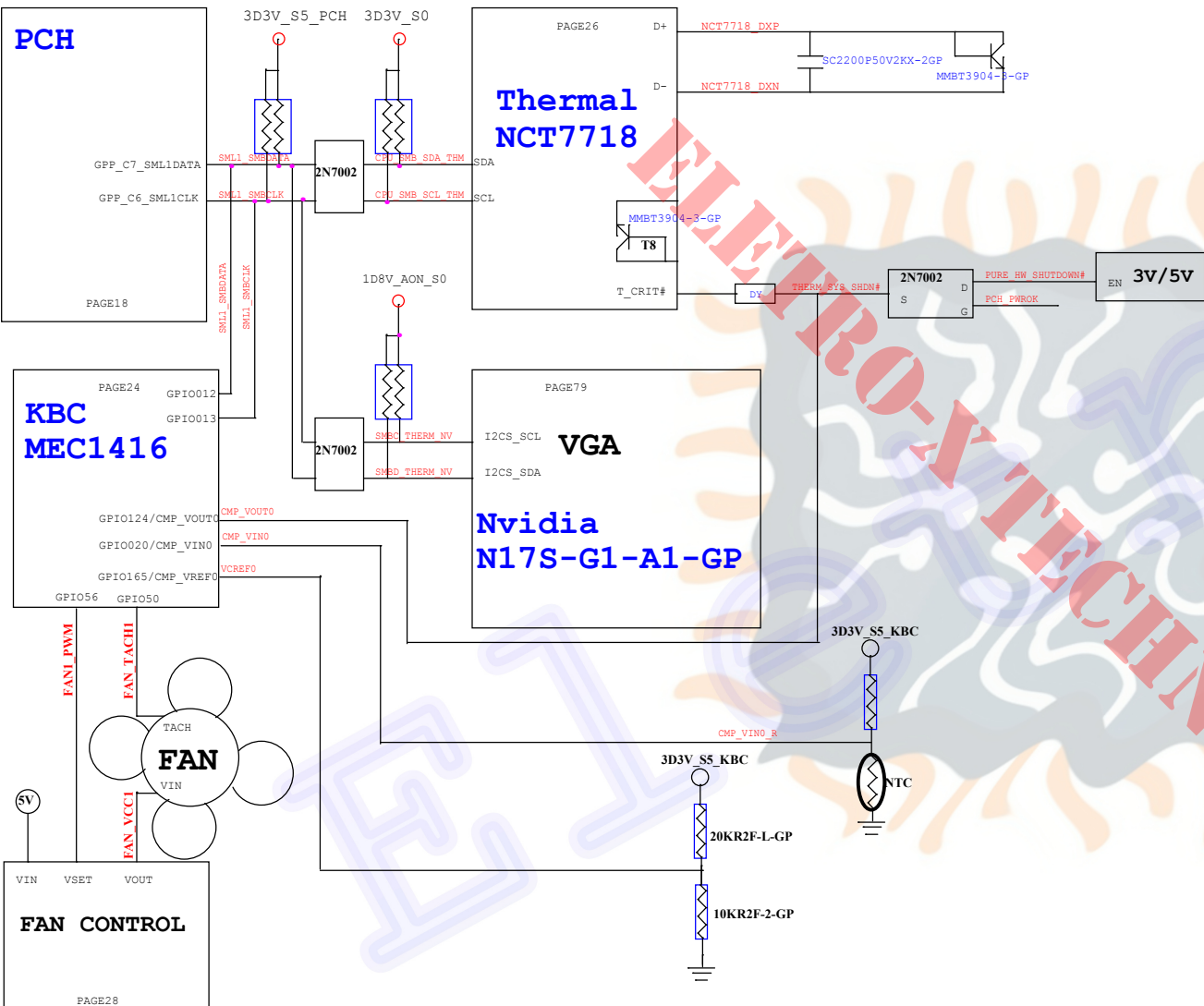
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PCH SMBus Block Diagram

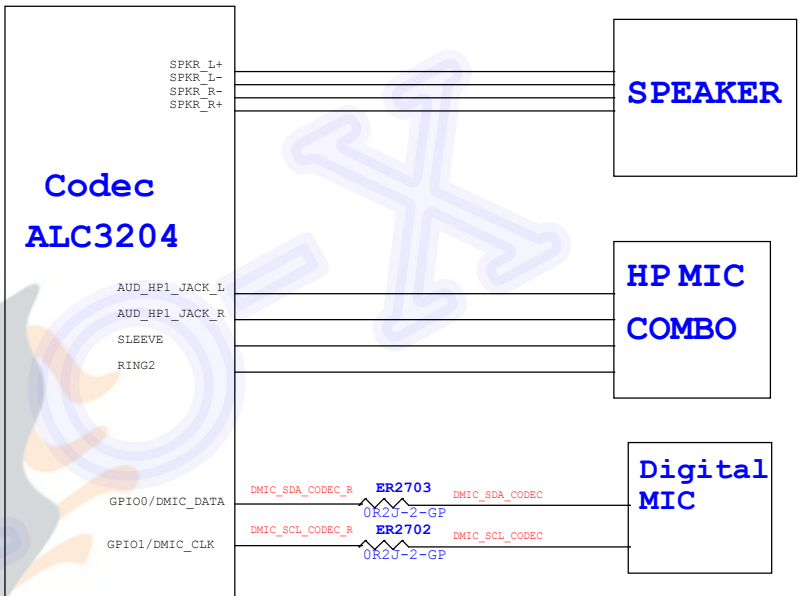
KBC SMBus Block Diagram

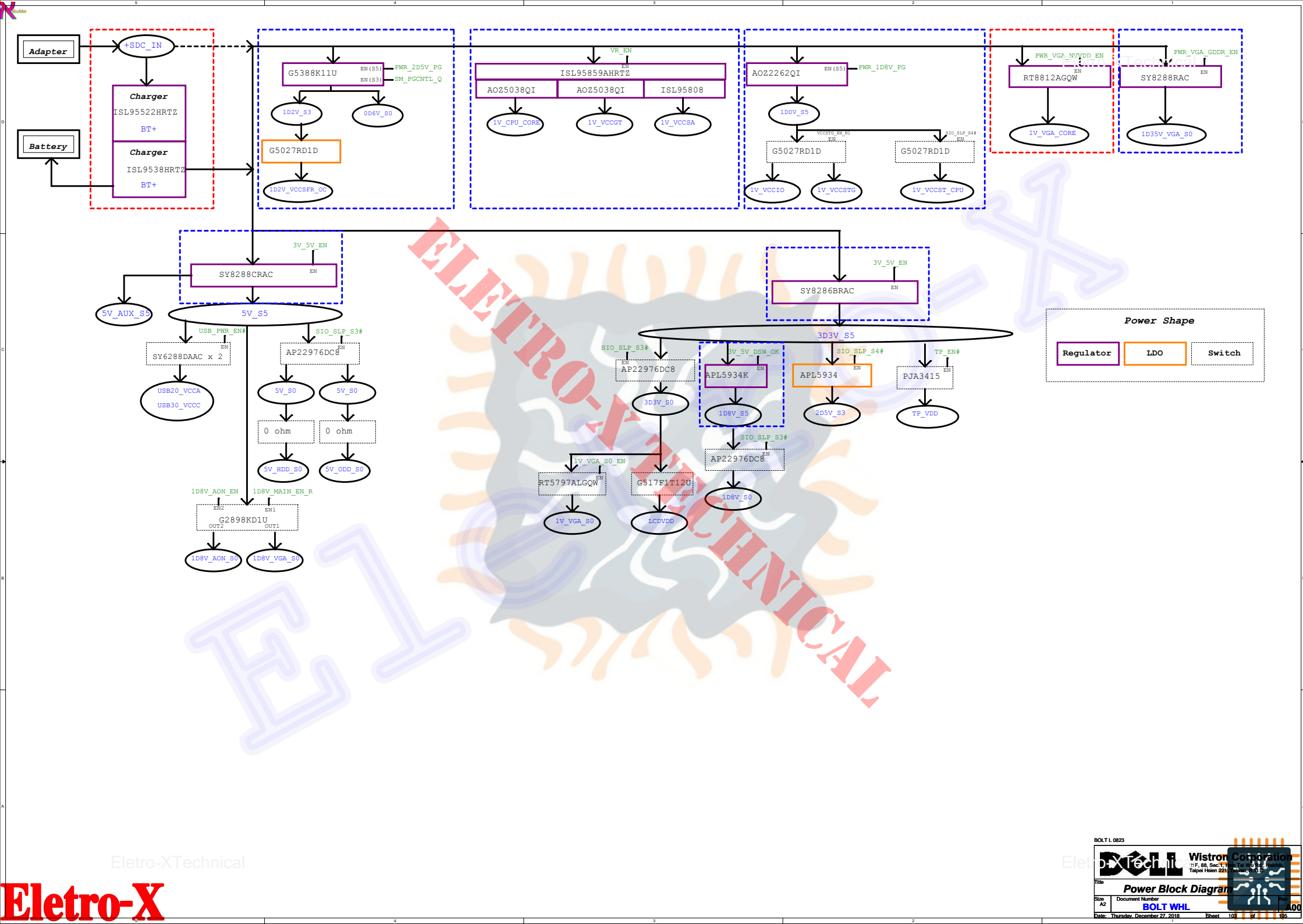


Thermal Block Diagram



Audio Block Diagram



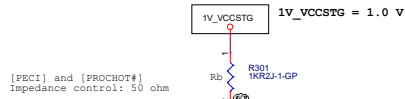


Main FUNC = CPU

24 PECL_CPU
24,44,46 PROCHOT#_CPU
55 TOUCH_PANEL_INTR#
24,65 TP_WAKE_KBC#
55 TOUCH_PANEL_PDR
17 H_CUPWRGD

55 CAM_EN

89 PCH_JTAG_TCK



TP_WAKE_KBC# Do Not Stuff 1 R319 2

(#575412) PROCHOT# Routing Guidelines

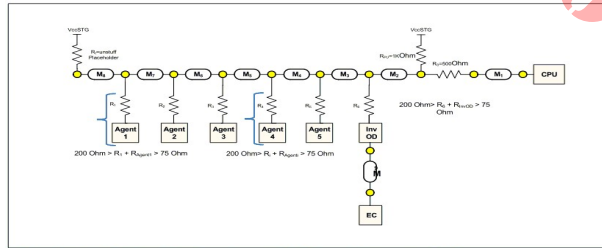


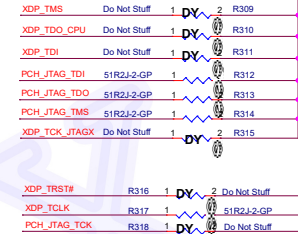
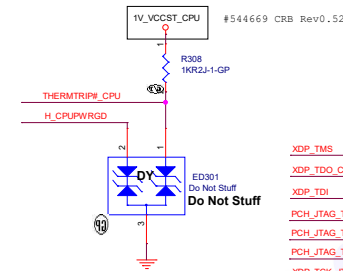
Table 7-11. PROCHOT# Routing Guidelines (Sheet 1 of 2)

Segment	Tline Type	Reference	Via Count	Max Length, mm		Max Length, Mils	
				Segment	Total	Segment	Total
M1	MS/SL/DSL	VSS	2	38	305	1496.06	12007.9
M2	MS/SL/DSL	VSS	2	279		10984.3	
M3	MS/SL/DSL	VSS	1	76		2992.13	
M4	MS/SL/DSL	VSS	1	76		2992.13	
M5	MS/SL/DSL	VSS	1	76		2992.13	
M6	MS/SL/DSL	VSS	1	76		2992.13	
M7	MS/SL/DSL	VSS	1	76		2992.13	
M8	MS/SL/DSL	VSS	1	8		341.96	
M9	MS/SL/DSL	VSS	2	254	254	10000	10000

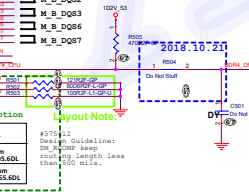
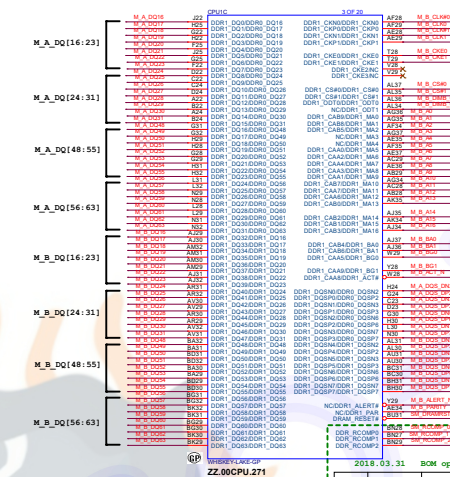
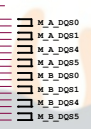
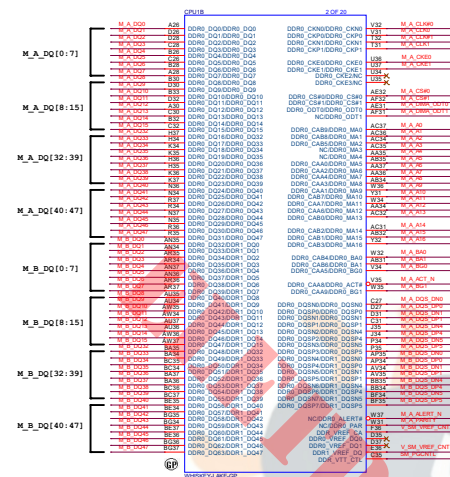
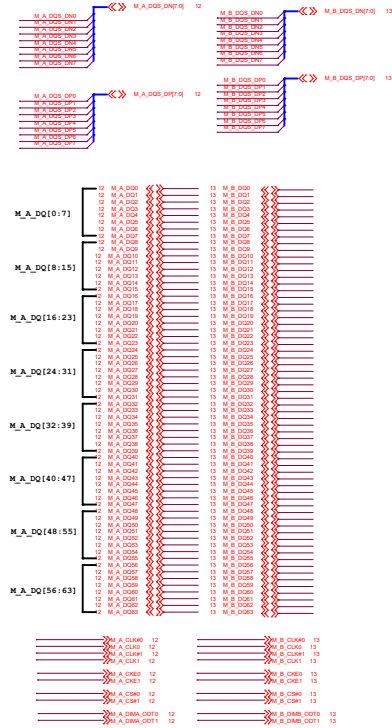
Topology Guidelines

Platform resistors values Rpu=1KΩ, Rs=500Ω, Ri+Ragent=75-200Ω, R6+Rinvod=75-200Ω

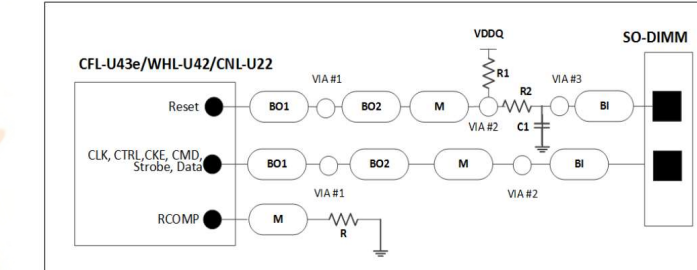
Platform resistors tolerances ± 5%



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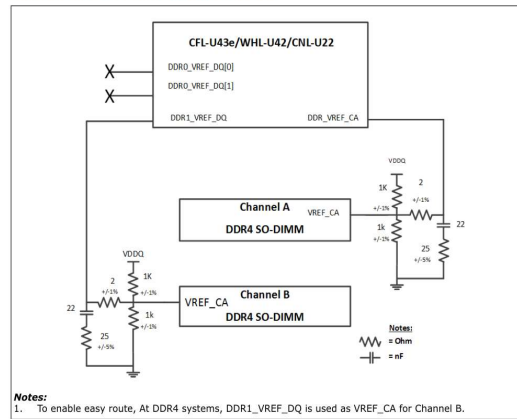
WHL U DDR4 SODIMM T3/8L Signals Topologies



Note: DRAM_RST C1 capacitor should not be installed

RCOMP (0/1/2)	M	US/SL	500	8000	15	20	25	CFL-U43e/ WHL-U42: 121/80.6/ 100
Reset	BO1	US	500	8000	3	6		R1=470 [5%] R2=0 C1=0.1uF (no stuff)
	BO2	SL	800-B01		3.5	12		
	M	SL		50	4	20		
	BI	US			4	20		

Figure 4-1. WHL U DDR4 SODIMM V_{REF-CA} Overview



Notes:
1. To enable easy route, At DDR4 systems, DDR1_VREF_DQ is used as VREF_CA for Channel B.



Main FUNC = CPU

Eletro-XTechnical

15 CFG3 <<>>
15 CFG4 <<>>

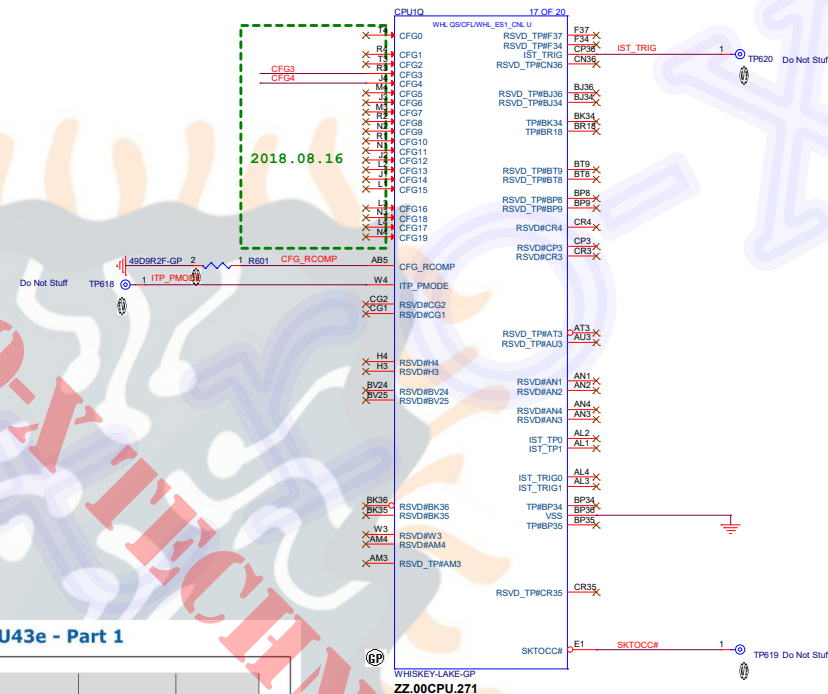


Figure 3-1. RCOMP Recommendation for WHL U42 and CFL U43e - Part 1

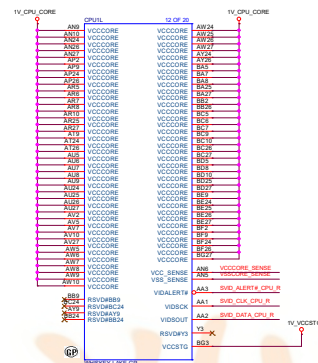
	LP3 DDR_RCOMP	DDR4 SODIMM DDR_RCOMP	DISP_RCOMP	CFG_RCOMP	PCIe_RCOMP_P/N	USB2_COMP
Board Rterm (ohm)	DDR_RCOMP[0]: 200Ω ±1% on pkg to VSS DDR_RCOMP[1]: 80.6Ω ±1% on pkg to VSS DDR_RCOMP[2]: 162Ω ±1% on pkg to VSS	DDR_RCOMP[0]: 121Ω ±1% on pkg to VSS DDR_RCOMP[1]: 80.6Ω ±1% on pkg to VSS DDR_RCOMP[2]: 100Ω ±1% on pkg to VSS	24.9Ω +/-1% to VCCIO	49.9Ω +/-1% to GND	100Ω +/-1% Differential	113Ω +/-1% to GND
Board Rdc (ohm)	n/a	n/a	<0.2	<0.5	<0.1	<0.5
DDR	x	x				
HDMI			x			
DP			x			
eDP			x			
CFG				x		
PCIe					x	
USB2						x

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Eletro-X

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46 VCCORE_SENSE
46 VCCORE_SENSE
46 SVID_DATA_CPU
46 SVID_CLK_CPU
46 SVID_ALERTN_CPU



Layout Note:
The total length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
Route the Alert signal between the Clock and the Data signals.

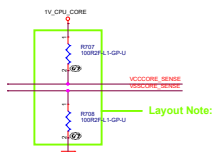
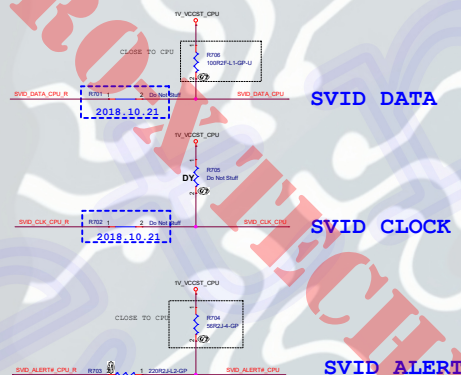


Figure 7-19. Routing Illustration for SVID Topology #575412

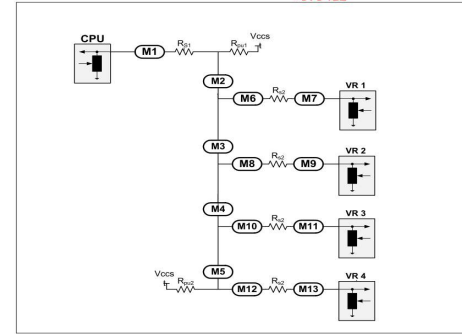
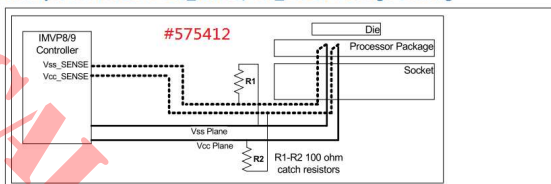


Figure above demonstrates Routing Illustration for SVID Topology, each trace from CPU to VR represents 3 signals: VIDSOUT, VIDSCK, VIDSALERT#.

SVID Signals	VIDSOUT, VIDSCK, VIDSALERT#
VIDSOUT platform resistors	Rpu1=100Ω, Rpu2=100Ω, Rs1=0Ω, Rs2=100Ω
VIDSCK platform resistors	Rpu1=Empty, Rpu2=45Ω, Rs1=0Ω, Rs2=49.9Ω
VIDSALERT# platform resistors	Rpu1=56Ω, Rpu2=Empty, Rs1=220Ω, Rs2=0Ω
Platform resistors tolerances	± 5%
Route ordering	When routing at minimum spacing route Alert between Data and Clock

12-3. Example of Processor Vcc_SENSE/Vss_SENSE Package Sensing



Package Sensing Recommendations

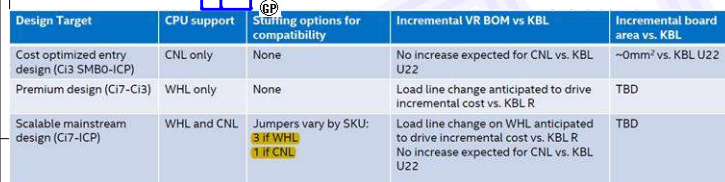
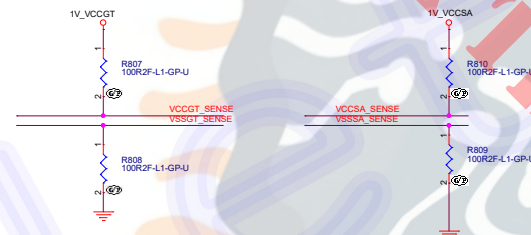
Power Rail Sense Line	R1, R2	Trace Impedance	Trace Length Match
Vcc_SENSE / Vss_SENSE	100Ω	50Ω	<25 mils
VccGT_SENSE / VssGT_SENSE			
VccSA_SENSE / VssSA_SENSE			
VccIO_SENSE / VssIO_SENSE ^[1]			

Note:
1. Does not apply when rails are merged.

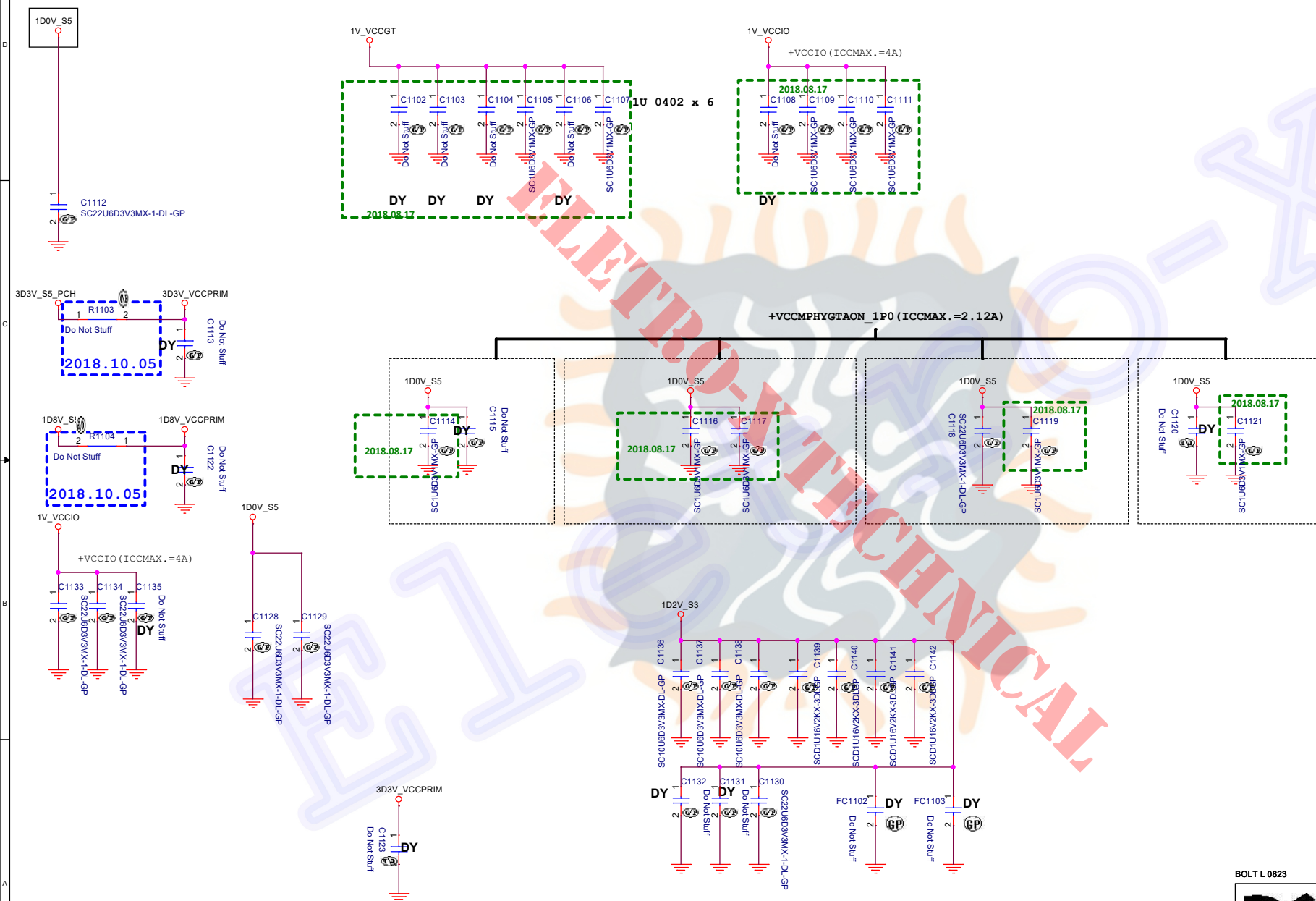
To minimize any stray noise pickup to the Vcc_SENSE/ Vss_SENSE lines

- Sense traces should be referenced to a solid ground plane
 - Avoid crossing over plane splits
 - Maintain 25-mil separation distance away from any other dynamic signals
- R1, R2 should be placed within 2 inches (50.8 mm) of the processor socket, minimizing any potential error due to Vcc_SENSE/Vss_SENSE line resistance.

Eletro-X



Pin Number	CFL-U43E	WHL E51 Netname	WHL E52 Netname
AA9	VCCGT	VCCGT	VCCCORE
AB10	VCCGT	VCCGT	VCCCORE
AB2	VCCGT	VCCGT	VCCCORE
AB8	VCCGT	VCCGT	VCCCORE
AB9	VCCGT	VCCGT	VCCCORE
AC8	VCCGT	VCCGT	VCCCORE
AD9	VCCGT	VCCGT	VCCCORE
AE10	VCCGT	VCCGT	VCCCORE
AE8	VCCGT	VCCGT	VCCCORE
AE9	VCCGT	VCCGT	VCCCORE
AF10	VCCGT	VCCGT	VCCCORE
AF2	VCCGT	VCCGT	VCCCORE
AF8	VCCGT	VCCGT	VCCCORE
AG8	VCCGT	VCCGT	VCCCORE
AG9	VCCGT	VCCGT	VCCCORE
AH9	VCCGT	VCCGT	VCCCORE
AJ10	VCCGT	VCCGT	VCCCORE
AJ8	VCCGT	VCCGT	VCCCORE
AK2	VCCGT	VCCGT	VCCCORE
AK9	VCCGT	VCCGT	VCCCORE
AL10	VCCGT	VCCGT	VCCCORE
AL8	VCCGT	VCCGT	VCCCORE
AL9	VCCGT	VCCGT	VCCCORE
AM8	VCCGT	VCCGT	VCCCORE
V2	VCCGT	VCCGT	VCCCORE
Y10	VCCGT	VCCGT	VCCCORE
Y8	VCCGT	VCCGT	VCCCORE



Layout Note:

```
1uF:
C1174 near N15
C1180 near K15
C1173 near AF20
C1172 near N18
C1175 near AB19
22uF :
C1182 C1184 near N15
10uF:
C1176 near N15
```


Main Func
= MEMORY

```

M_B_BA0 5
M_B_BA2 5
M_B_BA3 5
M_B_A4 5
M_B_A5 5
M_B_A6 5
M_B_A7 5
M_B_A8 5
M_B_A9 5
M_B_A10 5
M_B_A11 5
M_B_A12 5
M_B_A13 5
M_B_A14 5
M_B_A15 5
M_B_A16 5

M_B_BA0 5
M_B_BA1 5
M_B_BG0 5
M_B_BG1 5

M_B_CLK0 5
M_B_CLKR 5
M_B_CLKI 5
M_B_CLKIR 5

M_B_CKD 5
M_B_CKE1 5

M_B_CS0 5
M_B_CSRT 5

M_B_DIMB_COT
M_B_DIMB_COT

PCH_SMBDATA
PCH_SMBCLK

DDR4_DRAMSTR
M_B_ACT
M_B_ALERT

M_B_PARIT

V_M_SVREF_CN

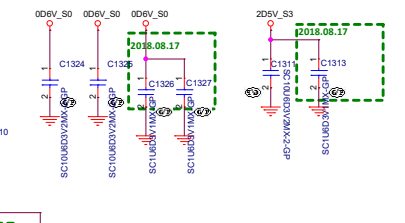
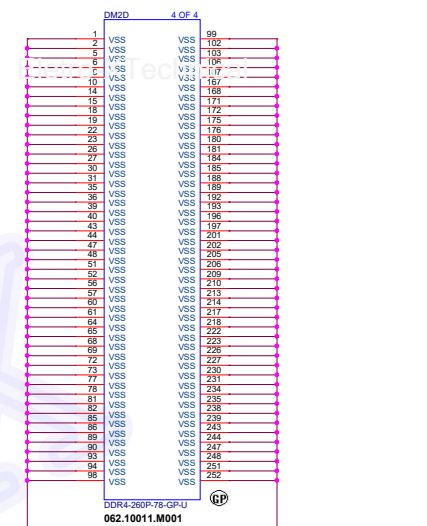
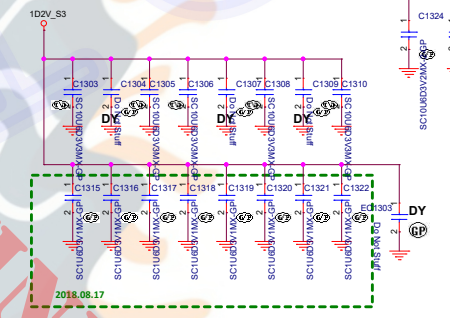
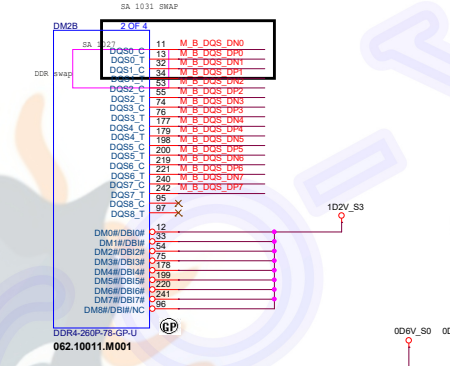
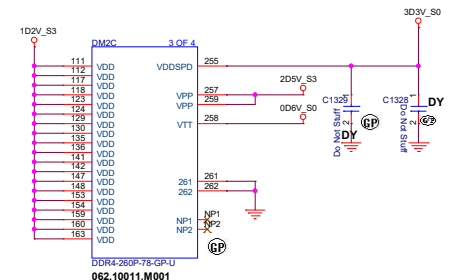
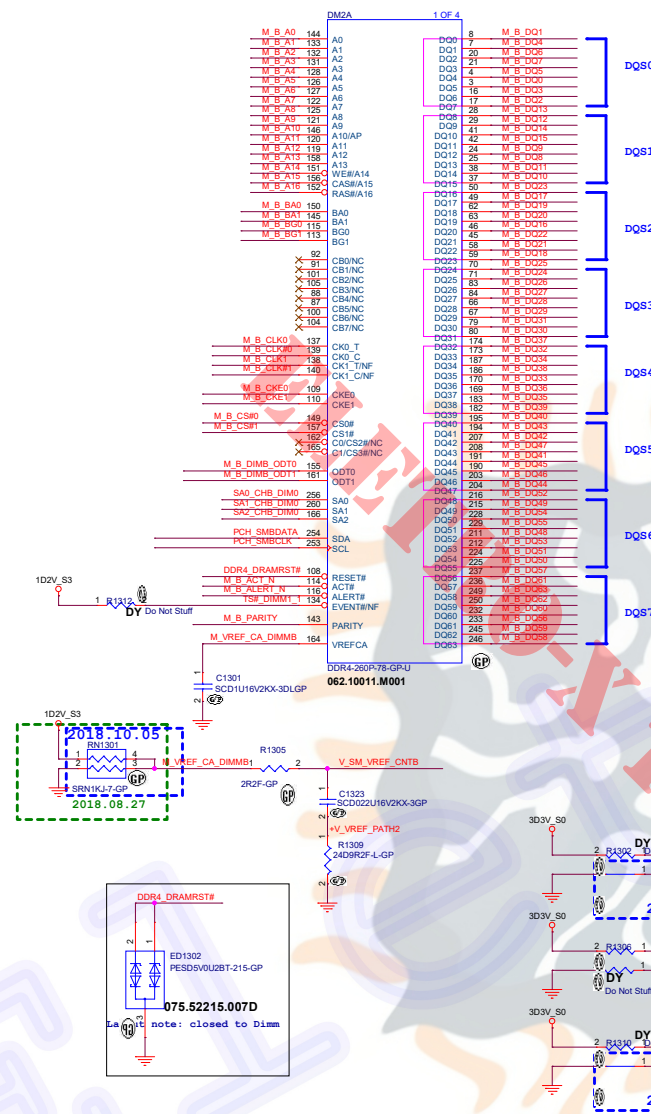
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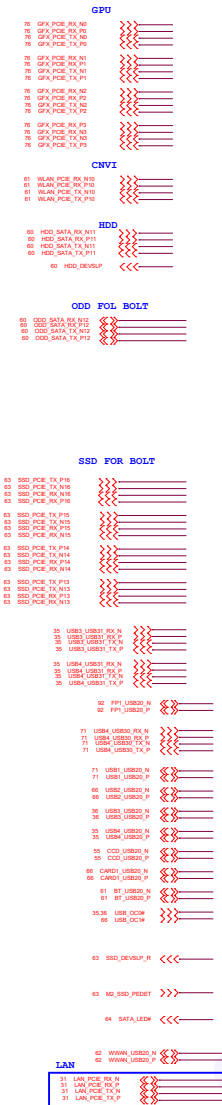
M.B.D00	5
M.B.D01	6
M.B.D02	7
M.B.D03	8
M.B.D04	9
M.B.D05	0
M.B.D06	1
M.B.D07	2
M.B.D08	3
M.B.D09	4
M.B.D10	5
M.B.D11	6
M.B.D12	7
M.B.D13	8
M.B.D14	9
M.B.D15	0
M.B.D16	1
M.B.D17	2
M.B.D18	3
M.B.D19	4
M.B.D20	5
M.B.D21	6
M.B.D22	7
M.B.D23	8
M.B.D24	9
M.B.D25	0
M.B.D26	1
M.B.D27	2
M.B.D28	3
M.B.D29	4
M.B.D30	5
M.B.D31	6
M.B.D32	7
M.B.D33	8
M.B.D34	9
M.B.D35	0
M.B.D36	1
M.B.D37	2
M.B.D38	3
M.B.D39	4
M.B.D40	5
M.B.D41	6
M.B.D42	7
M.B.D43	8
M.B.D44	9
M.B.D45	0
M.B.D46	1
M.B.D47	2
M.B.D48	3
M.B.D49	4
M.B.D50	5
M.B.D51	6
M.B.D52	7
M.B.D53	8
M.B.D54	9
M.B.D55	0
M.B.D56	1
M.B.D57	2
M.B.D58	3
M.B.D59	4
M.B.D60	5

M_B_QQS_DN0
M_B_QQS_DN1
M_B_QQS_DN2
M_B_QQS_DN3
M_B_QQS_DN4
M_B_QQS_DN5
M_B_QQS_DN6
M_B_QQS_DN7

M_B_QQS_DN[7:0] 5

Diagram showing the connection of M_B_DQS_DP0 through M_B_DQS_DP7 to a bus labeled M_B_DQS_DP[7:0] 5.





#543016:
220 nF nominal capacitors are recommended for Gen 3.
400 nF nominal capacitors are recommended for Gen 2.

2018.08.16
2018.08.02



#543559: The xHCI controller supports USB Debug port on all USB3.0 capable ports.

Eleto-X Technical

USB 2.0 Table

Pair	Device
1	USB1 (USB Charger)
2	IO board USB2.0
3	USB2 COM
4	TYPE-C USB/ I2C MIX
5	Finger Print
6	CAMERA
7	Card Reader
8	WLAN
9	Touch Panel
10	WLAN (BT)

Overcurrent Protection #575412

Whiskey Lake PCH has implemented programmable USB Overcurrent signals. The 4 overcurrent pins are to be shared across the USB 2.0 ports and USB 3.1 ports. This allows the platform designer flexibility in routing of the OC pins and allows for unused pins to be configured as GPIOs.

It is the responsibility of system software (BIOS) to program the overcurrent registers of the given USB controller correctly and to make sure that each USB port is protected by only one overcurrent pin. Operation with more than one overcurrent pin mapped to a port is undefined.

#575412
USB ID and USB3_SSRX signals are not needed for USB Type-C implementation with Type-C Port Controller (TPC).

Figure 6-1. High Speed I/O (HSIO) Lane Multiplexing in CNL PCH-LP

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #6	PCIe #7	PCIe #8	PCIe #9	PCIe #10	PCIe #11	PCIe #12	PCIe #13	PCIe #14	PCIe #15	PCIe #16
High Speed I/O (HSIO) Type and Lane	PCIe #1	PCIe #2	PCIe #3	PCIe #4	PCIe #5	PCIe #6	GbE	GbE	GbE	SATA 0	SATA 1a	GbE	GbE	SATA 1b	SATA 2	SATA 2
Intel® RST Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	Yes	Yes	Yes	Yes	Yes	Yes	Yes

6.4.1 PCH PCI Express* Device Down Guidelines

Figure 6-3. PCH PCI Express* Device Down at 2.5, 5, and 8 GT/s Topology

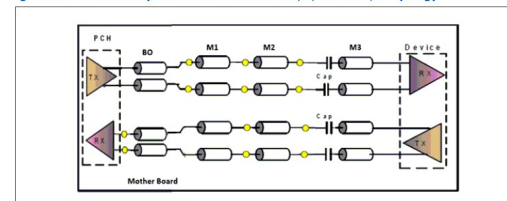


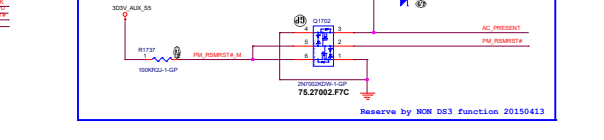
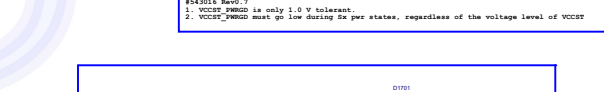
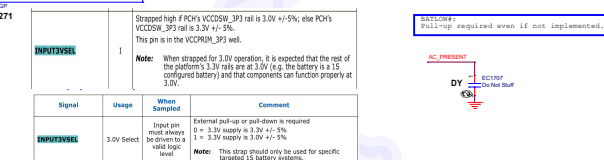
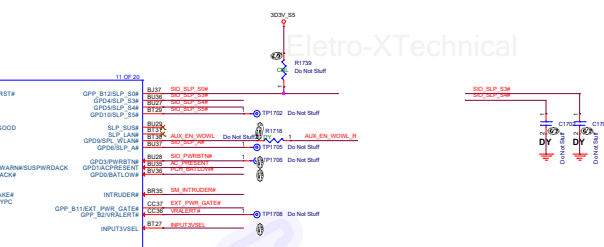
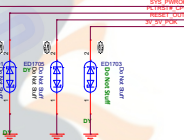
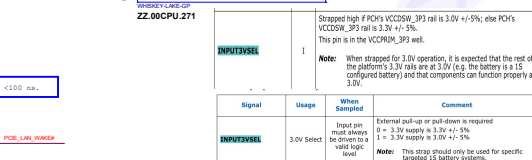
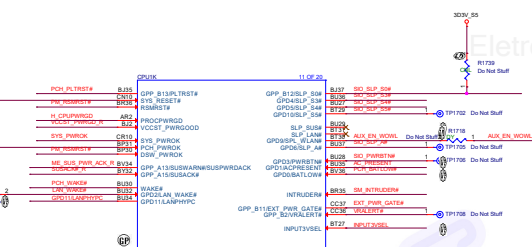
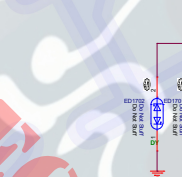
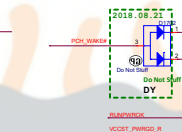
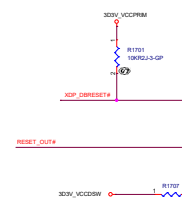
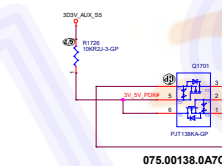
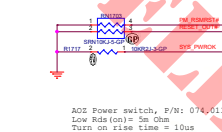
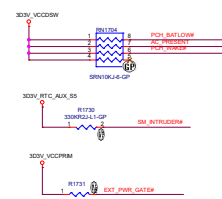
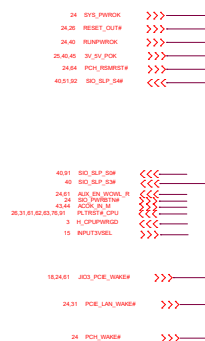
Table 6-6. PCH PCI Express* Device Down Routing Guidelines (Sheet 1 of 2)

Parameter	Segment	Stack-up (MS/SL/DSL)	Units	2.5 GT/s Routing	5 GT/s Routing	8 GT/s Routing
Reference Plane	BO, M1, M2, M3	MS/SL/DSL	NA	GND	GND	GND
Break-Out Max Length	BO	MS/SL/DSL	mm(mils)	15.2(598.42)	15.2(598.42)	15.2(598.42)
Post-AC Capacitor Max Length	M3	MS	mm(mils)	8(314.96)	8(314.96)	8(314.96)

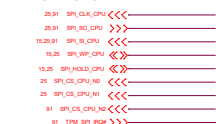
Figure 3-1. RCOMP Recommendation for WHL U42 and CFL U43e - Part 1

	LP3 DDR_RCOMP	DORA SODIMM DDR_RCOMP	DISP_RCOMP	CFG_RCOMP	PCIe_RCOMP_P/N	USB2_COMP
Board Rterm (ohm)	DDR_RCOMP[0]: 2000 ±1% on pkg to VSS DDR_RCOMP[1]: 80.60 ±1% on pkg to VSS DDR_RCOMP[2]: 1620 ±1% on pkg to VSS	DDR_RCOMP[0]: 1210 ±1% on pkg to VSS DDR_RCOMP[1]: 80.60 ±1% on pkg to VSS DDR_RCOMP[2]: 1000 ±1% on pkg to VSS	24.90 ±1% to VCCO	49.90 ±1% to GND	100Ω ±1% Differential	118Ω ±1% to GND
Board Rdc (ohm)	n/a	n/a	<0.2	<0.5	<0.1	<0.5
DDR	X	X				
HDMI			X			
DP			X			
eDP			X			
CFG				X		
PCIe					X	
USB2						X

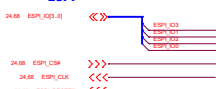
Eleto-X Technical



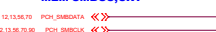
SPI ROM&TPM



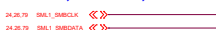
ESPI



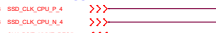
MEM SMBUS,CRT



KBC,Thermal,Fan,GPU



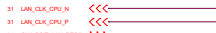
M.2 SSD



GPU



LAN



WWAN



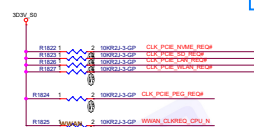
CNVI



RTCRST



STRAP



FREE FALL SENSOR



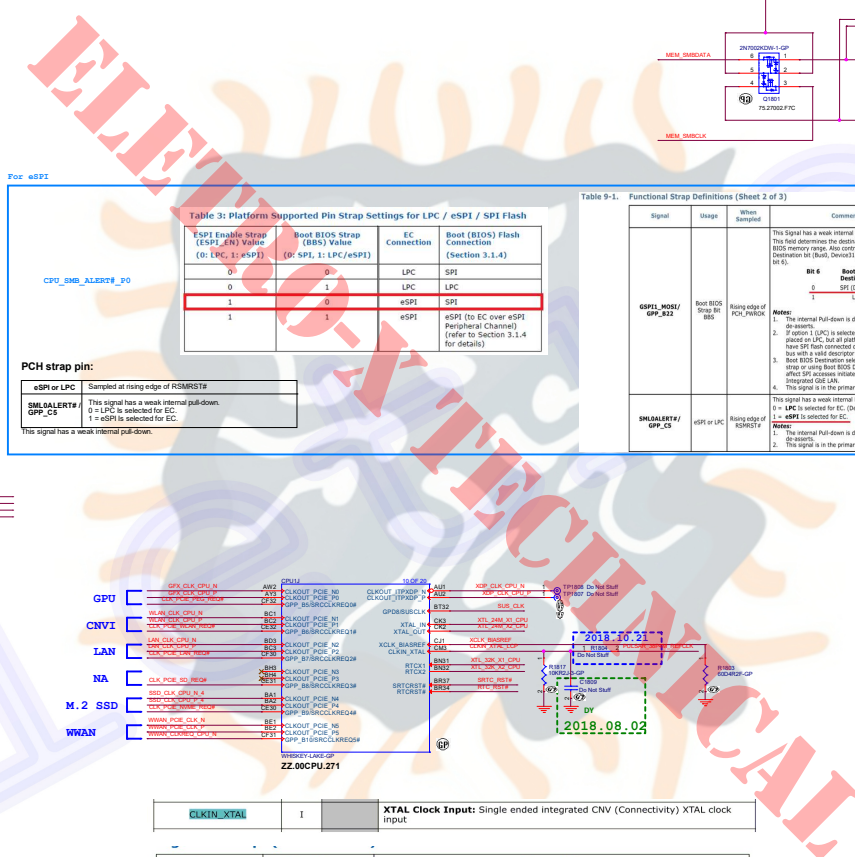
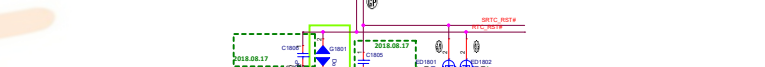
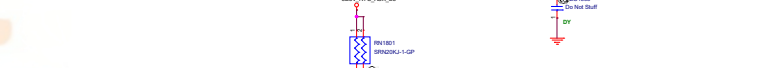
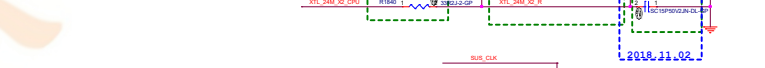
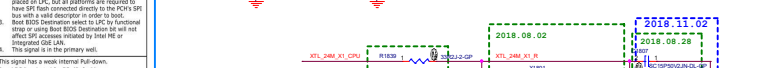
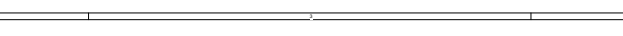
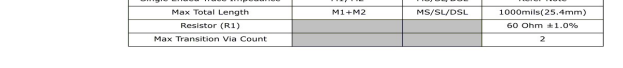
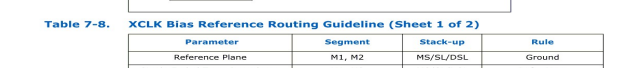
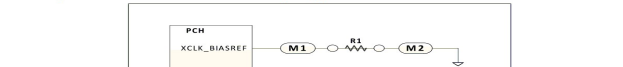
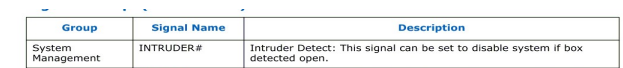
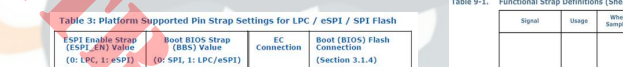
STRAP



STRAP



CPU TYPE	CN(L100M-BM)	WH(L100M)
But-L(TPM)	64.10R05.4DL	63.5R13A.1DL
But (non-TPM)	63.5R13A.1DL	64.4R0R5.4DL



For eSPI

Table 3: Platform Supported Pin Strap Settings for LPC / eSPI / SPI Flash			
eSPI Enable Strap (eSPI_EN) Value (0: LPC, 1: eSPI)	Boot BIOS Strap (BIOS) Value (0: SPI, 1: LPC/eSPI)	EC Connection	Boot (BIOS) Flash Connection (Section 3.1.4)
0	0	LPC	SPI
0	1	LPC	LPC
1	0	eSPI	LPC
1	1	eSPI	eSPI (to EC over eSPI Peripheral Channel) (refer to Section 3.1.4 for details)

Signal	Usage	When Sampled	Comment
eSPI_MOSI / GPP_R23	Root BIOS Strap	Rising edge of PCH_PWDN	This signal has a weak internal pull-down. The first determines the destination of accesses to the BIOS memory map. Also, connections using Root BIOS Strap are required to have SPI flash connected directly to the PCH's SPI pin with a valid destination in SPI flash.
SHALERT# / GPP_CS	eSPI or LPC	Rising edge of eSPI#	This signal has a weak internal pull-down. 1. eSPI is selected for EC. (Default) 2. eSPI is selected for EC. This signal is in the primary well.

For eSPI

eSPI or LPC | Sampled at rising edge of RSMRST#
This signal has a weak internal pull-down.
0 = LPC is selected for EC.
1 = eSPI is selected for EC.
This signal has a weak internal pull-down.

For eSPI

For eSPI

For eSPI

For eSPI

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For eSPI

CLIN_XTAL	I	XTAL Clock Input: Single ended integrated CNV (Connectivity) XTAL clock input
-----------	---	---

Group	Signal Name	Description
System Management	INTRUDER#	Intruder Detect: This signal can be set to manage system if box detected open.
RTC	RTCRST#	Secondary RTC Reset: This signal resets the manageable register bits in the RTC well when the RTC battery is removed.
RTC	RTCRST#	RTC Reset: When asserted, this signal resets register bits in the RTC well.

Figure 7-11. XCLK Bias Reference Topology

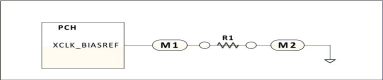
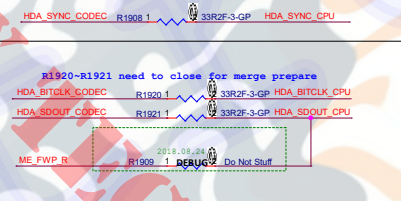
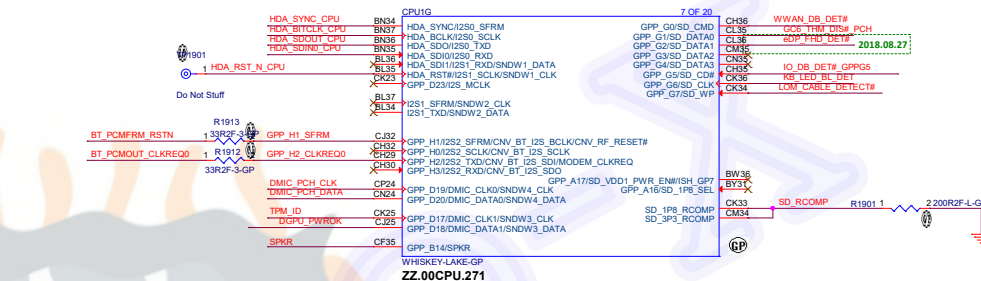
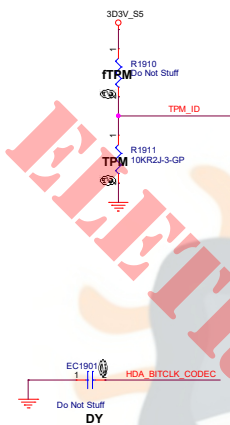


Table 7-8. XCLK Bias Reference Guideline (Sheet 1 of 2)

Parameter	Segment	Stack-up	Rule
Reference Plane	M1, M2	MS/SL/DSL	Ground
Single Ended Trace Impedance	M1, M2	MS/SL/DSL	Refer Note
Max. Total Length	M1+M2	MS/SL/DSL	1000mm(25.4mm)
Resistor (R1)			60 Ohm ±1.0%
Max Transition Via Count			2

21,24,62 WWAN_DB_DET#>>>-----

These two signals have weak internal pull-down.



	SD_RCOMP_1P8	SD_RCOMP_3P3	EMMC_RCOMP	XCLK_BIASREF	CNV_WT_RCOMP	PCH_OPIRCOMP	PROC_POPIRCOMP
Board Rterm (ohm)	200Ω +/-1% to GND	200Ω +/-1% to GND	200Ω +/-1% to GND	60Ω +/-1% to GND	150Ω +/-1% to GND	49.9Ω +/-1% to GND	49.9Ω +/-1% to GND
	Notes: SD_RCOMP_1P8, SD_RCOMP_3P3 and EMMC_RCOMP can be merged into one 200Ω +/-1% to GND resistor. Routing each of them to individual 200Ω +/-1% to GND resistor is an option too.						
Board Rdc (ohm)	<0.1	<0.1	<0.1	<0.5	<0.5	<0.2	<0.2
SD3	X	X					
EMMC			X				
POPI						X	X
XTAL				X			
CNV1_DPHY					X		



61 BLUETOOTH_EN <<<
61 WIFI_RF_EN <<<

20,64 PWR_BD_DET# >>>

15 GPP_H21 >>>
15 GPP_H23 >>>
15 GPD_7 >>>

40 GPPC_H18_VCCIO_LPM <<<

18 PROJECT_ID0 <<<

CNvi TX for wifi

61 CNV_WT_CLK_DP >>>
61 CNV_WT_CLK_DN >>>
61 CNV_WT_DP0 >>>
61 CNV_WT_DP1 >>>
61 CNV_WT_DN0 >>>
61 CNV_WT_DN1 >>>

CNvi RX for wifi

61 CNV_WR_CLK_DP >>>
61 CNV_WR_CLK_DN >>>
61 CNV_WR_DP0 >>>
61 CNV_WR_DP1 >>>
61 CNV_WR_DN0 >>>
61 CNV_WR_DN1 >>>

LTE COEX

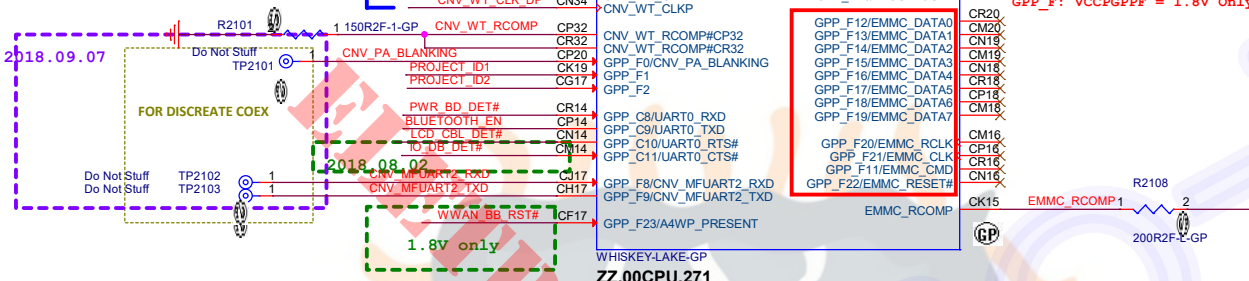
19,24,62 WWAN_DB_DET# >>>

62 WWAN_BB_RST# <<<

20,55 LCD_CBL_DET# >>>

66 IO_DB_DET# >>>

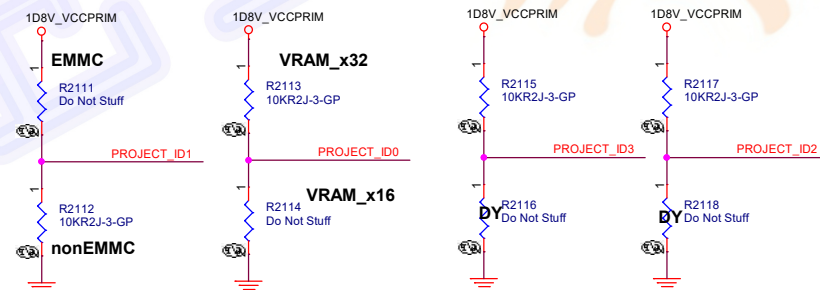
CNVI FOR WIFI



WWAN_BB_RST

Power Management States for Modern connected standby platform

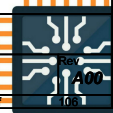
System States	USB device States	PCIe Device States	PCIe Link States	PERST#	PEWAKE#	CLKREQ#	SB_RESET#	Notes
50	D0	D0	L0, L3.2	H	H	L0, L3.2 : H	H	
	D2	D3cold	L2	L	H	H	H	
50n	D2	D3cold	L2	L	H	H	H	
	D3cold	D3cold	L3	-	-	-	L	Power is removed from modem
54	D2	D3cold	L2	L	H	H	H	
	D3cold	D3cold	L3	-	-	-	L	
55	D3cold	D3cold	L3	-	-	-	L	Power is removed from modem

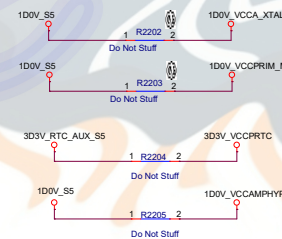
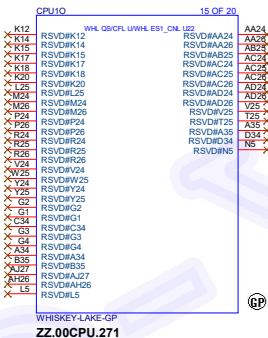


BOLT.L 0823

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

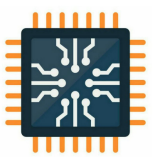
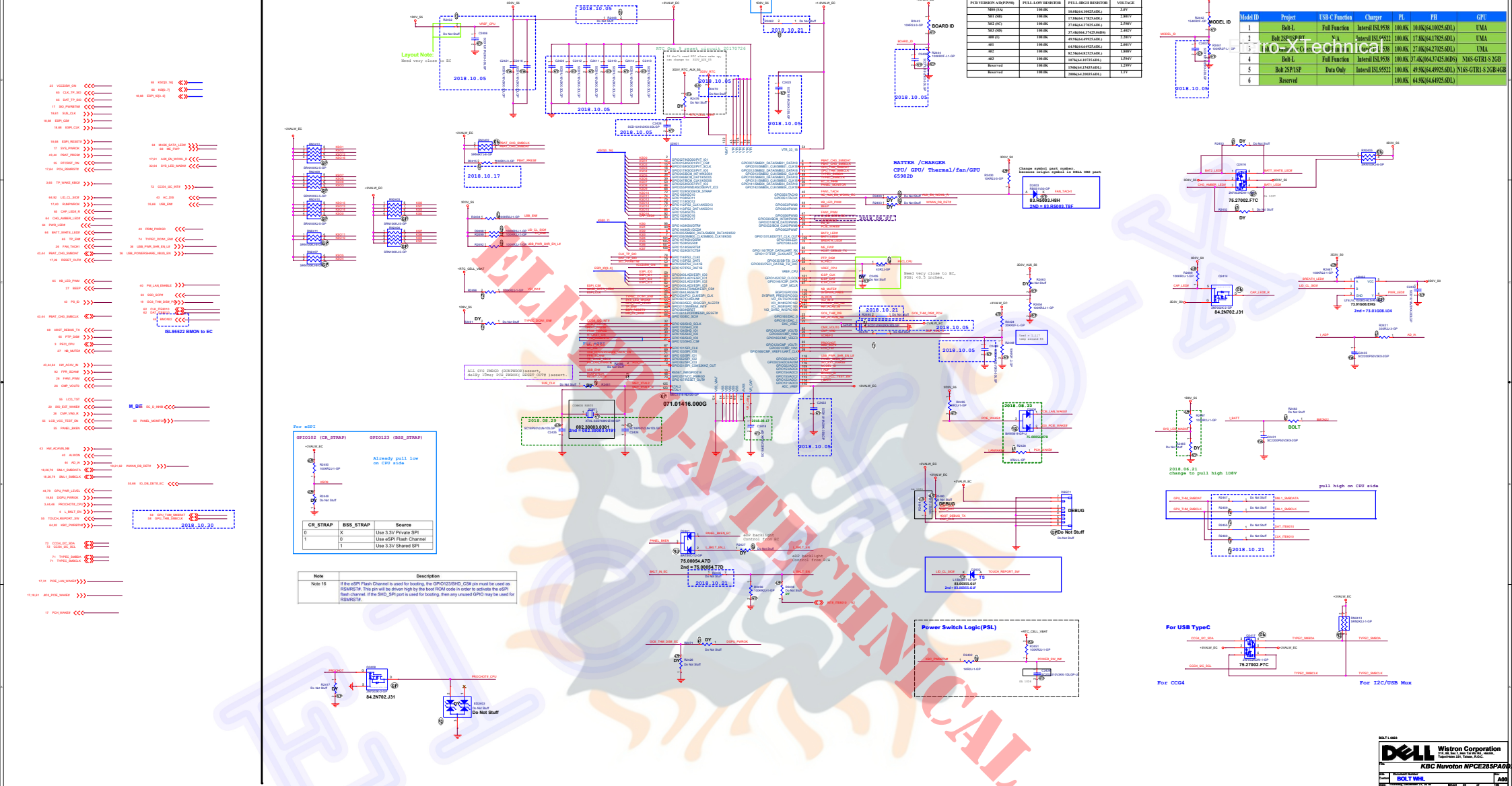
Title: CPU (POWER1)
Size: A3 Document Number: RogueOne 13"
Date: Thursday, December 27, 2018 Sheet 21 of 21



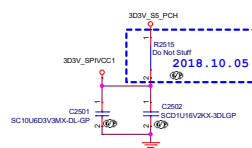


CPU1T		CPU2T	
N6	V5S	CF23	V5S
B37	V5S	V5S	V5S
C83	V5S	B630	V5S
C85	V5S	V229	V5S
B5	V5S	W16	V5S
C86	V5S	B631	V5S
P3	V5S	C3	V5S
B7	V5S	V27	V5S
C87	V5S	W27	V5S
B3	V5S	V24	V5S
P36	V5S	V37	V5S
C87	V5S	C033	V5S
B3	V5S	W7	V5S
B410	V5S	B13	V5S
C111	V5S	C07	V5S
B3	V5S	B936	V5S
B428	V5S	V37	V5S
P7	V5S	B4	V5S
B3	V5S	C21	V5S
C20	V5S	V27	V5S
V27	V5S	V27	V5S
B37	V5S	B625	V5S
C22	V5S	V20	V5S
C75	V5S	B628	V5S
B33	V5S	V3	V5S
C28	V5S	C14	V5S
C3	V5S	V37	V5S
B36	V5S	B128	V5S
C31	V5S	C19	V5S
V36	V5S	V7	V5S
B4	V5S	B129	V5S
B3	V5S	B102	V5S
B22	V5S	C28	V5S
C1	V5S	C35	V5S
C127	V5S	C33	V5S
C121	V5S	C35	V5S
B29	V5S	B119	V5S
C14	V5S	C216	V5S
V33	V5S	B118	V5S
B32	V5S	C216	V5S
C024	V5S	B016	V5S
B3	V5S	C14	V5S
C025	V5S	B122	V5S
B3	V5S	B120	V5S
C3	V5S	B121	V5S
C33	V5S	B114	V5S
C3	V5S	B115	V5S
B28	V5S	C14	V5S
C026	V5S	C14	V5S
C35	V5S	C224	V5S
B33	V5S	U2	V5S
C3	V5S	U2	V5S
V26	V5S	U2	V5S
B135	V5S	U2	V5S
C3	V5S	U2	V5S
V27	V5S	B4E	V5S
B036	V5S	B4	V5S
C1	V5S	B4	V5S
V3	V5S	B4	V5S
B3	V5S	B4	V5S
C14	V5S	B4	V5S
B3	V5S	B4	V5S
C19	V5S	C3	V5S
B3	V5S	C3	V5S
B29	V5S	CMM	V5S
CF2	V5S	C3	V5S
CF3	V5S	C3	V5S
V36	V5S	C3	V5S
B27	V5S	C3	V5S

WHISKEY-LAKE-GP
ZZ.00CPU.271

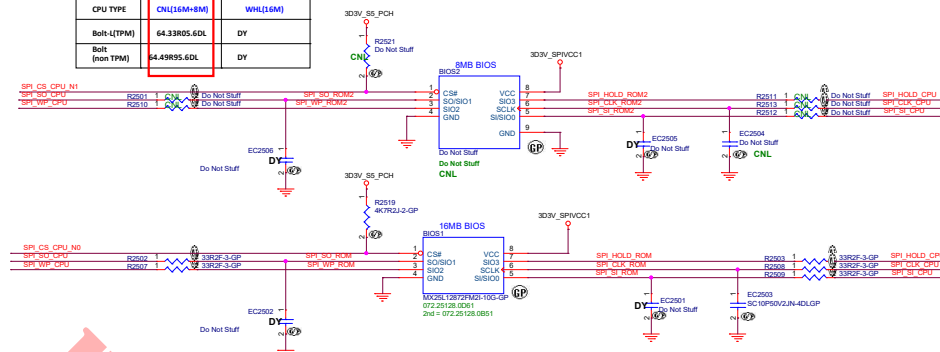


18	SPI_CS_CPU_N1	>>>
18	SPI_CS_CPU_N0	>>>
15,18	SPI_HOLD_CPU	<<<
24	RTC_RST_ON	>>>
	53_5V_SW_DSW_OK	<<<
18,91	SPI_SO_CPU	<<<
15,18	SPI_WP_CPU	<<<
18,91	SPI_CLK_CPU	>>>
15,18,91	SPI_SI_CPU	>>>
15,20	RTC_DET#	<<<
24	VCCDSW_ON	>>>
17,40,45	3V_5V_POK	>>>

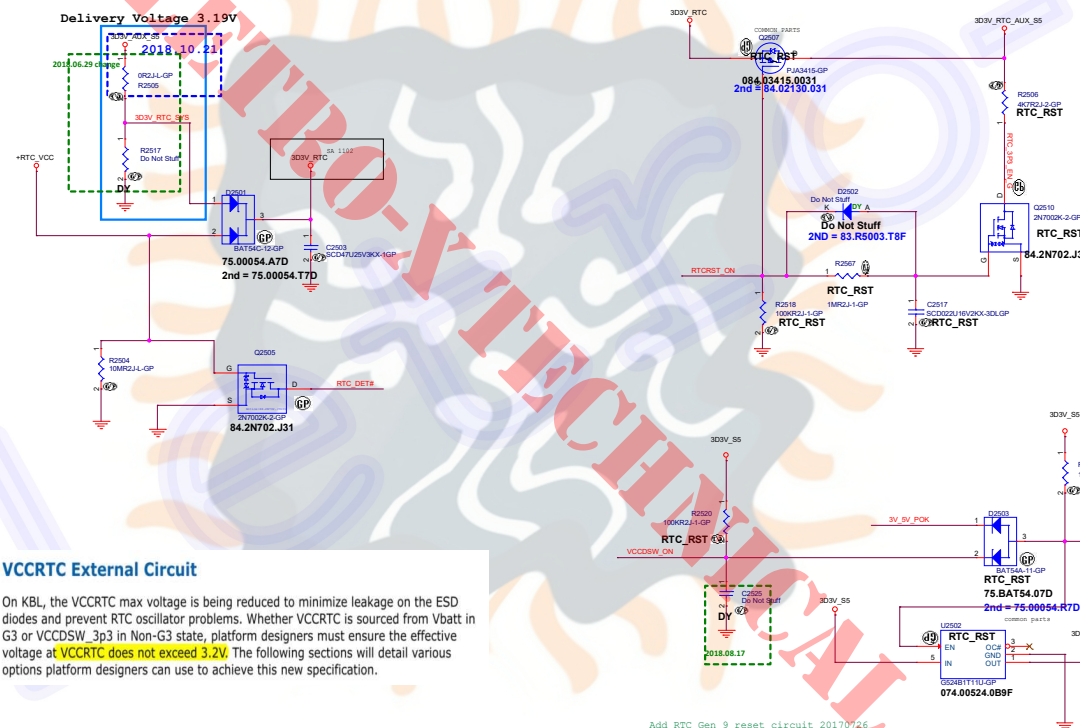


R2502/R2507/R2503/R2508/R2509		
CPU TYPE	CNL(16M+8M)	WHL(16M)
Bolt-L(TPM)	64.33R05.6DL	64.49R95.6DL
Bolt (non TPM)	064.49R95.56D1	63.R0034.L0L

R2501/R2510/R2511/R2513/R2517		
CPU TYPE	CNL(16M+8M)	WHL(16M)
Bolt-L(TPM)	64.33R05.6DL	DY
Bolt (non TPM)	64.49R95.6DL	DY



Main Func = RTC

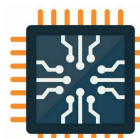


29.2.1 VCCRTC External Circuit

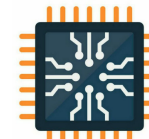
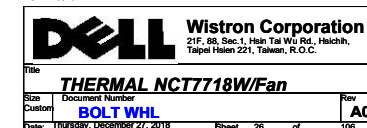
On KBL, the VCCRTC max voltage is being reduced to minimize leakage on the ESD diodes and prevent RTC oscillator problems. Whether VCCRTC is sourced from Vbatt in G3 or VCCDSW_3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.2V. The following sections will detail various options platform designers can use to achieve this new specification.

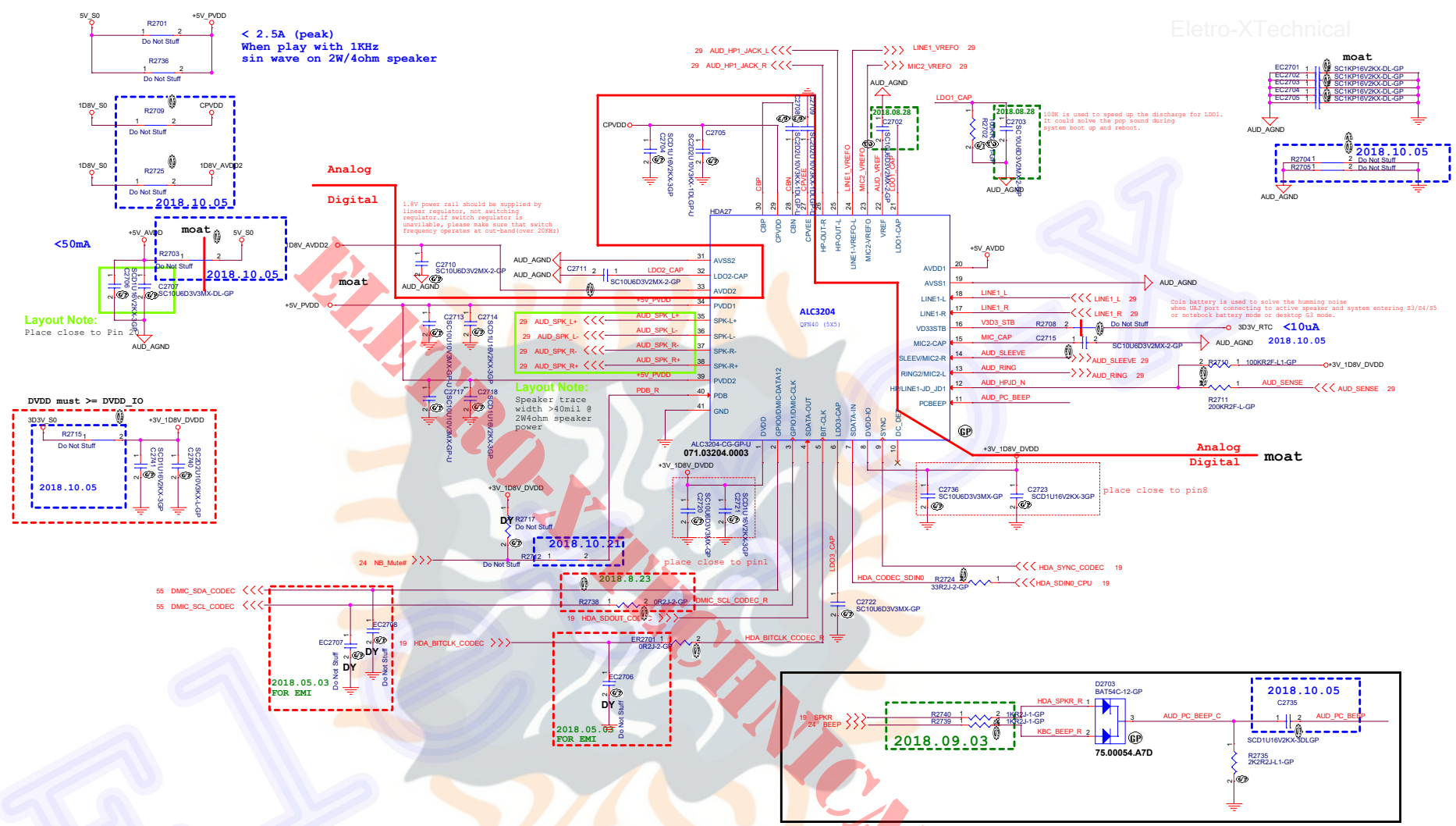
Add RTC Gen 9 reset circuit 20170726

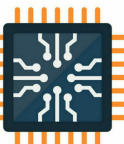
BOLT L 082



Eletro-X





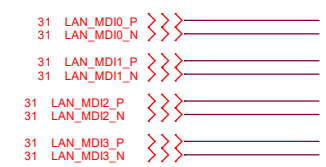


Main Func = LAN

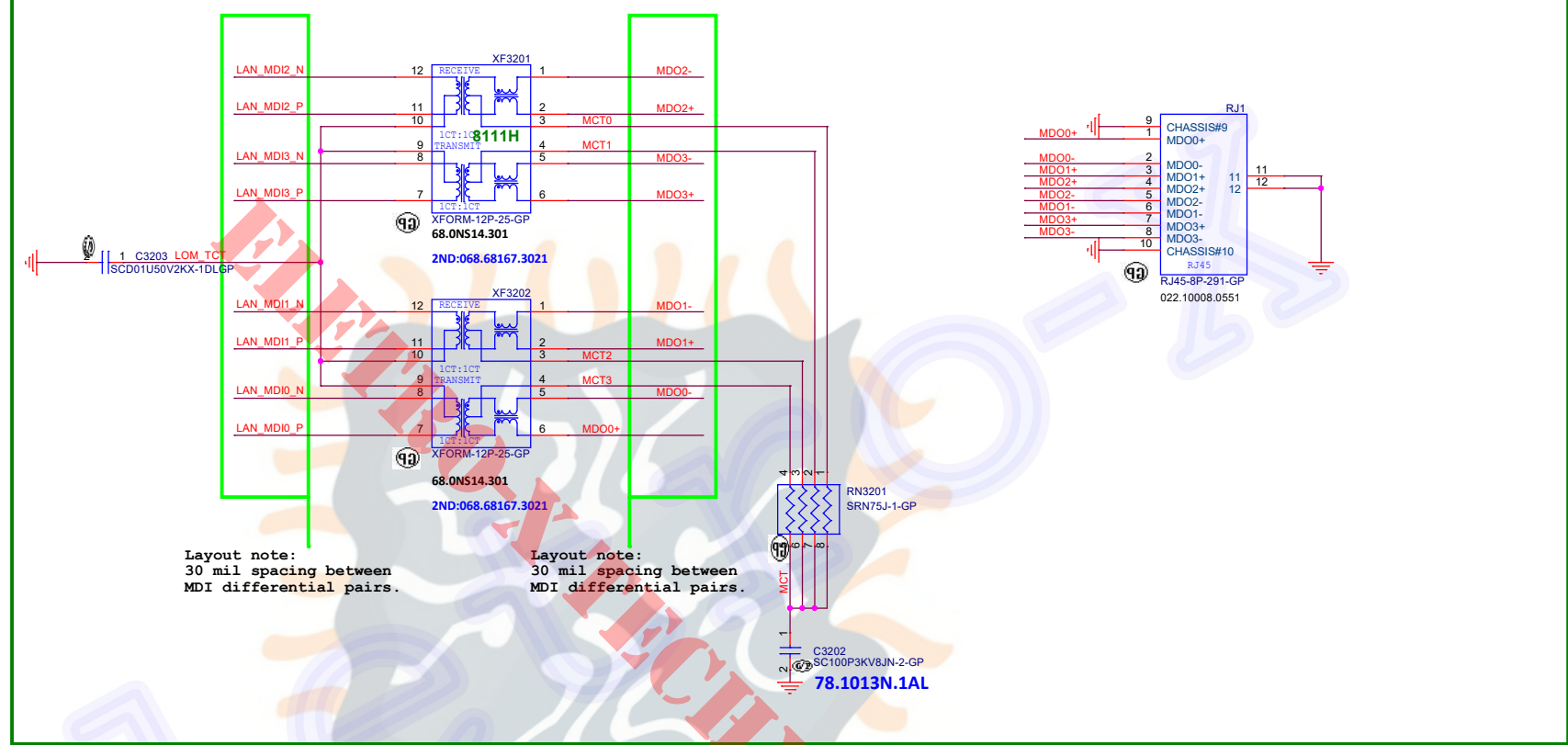
LAN TransFormer (10/100/1000M & 10/100M co-lay)

Eleto-XTechnical

MDI

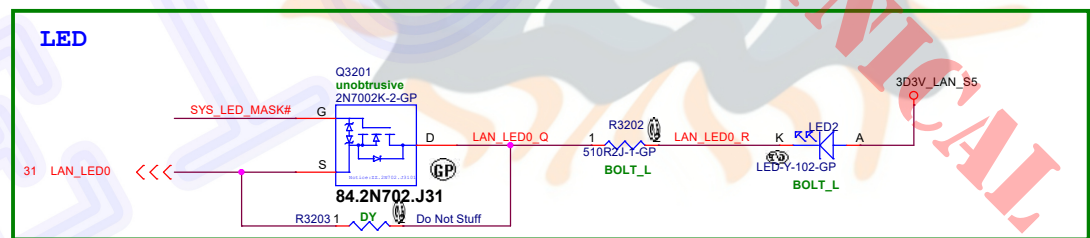


24,64 SYS_LED_MASK# >>>

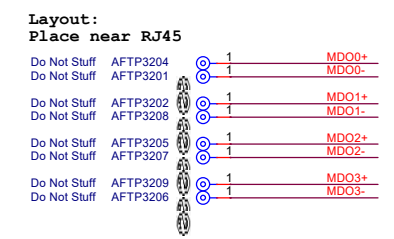


LED

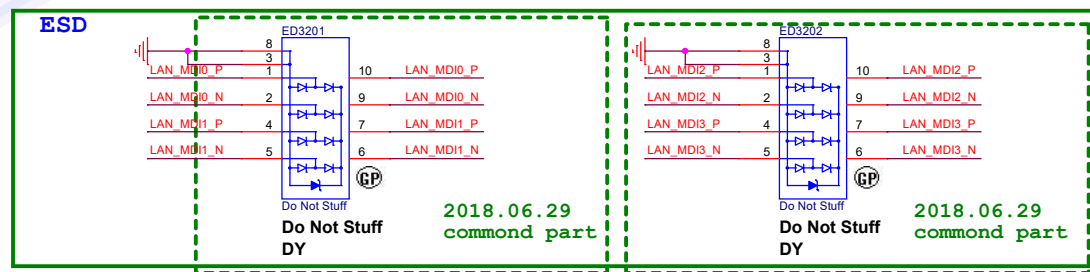
Green LED Status:
Blinking:Data transmit (10/100/1000)
Always Turn On: Network Connection exist
Turn Off: No network connection exist



TEST PAD



ESD



BOLT L 0823

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsin 221, Taiwan, R.O.C.

Title: Eleto-X
Size: A3
Document Number: BOLT WHL
Date: Thursday, December 27, 2018
Sheet: 32 of 32

XFOM&RJ45

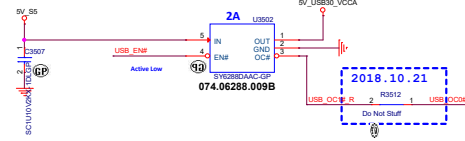
Yehulder Main Func = USB 3.0

USB Power Switch Enable

24,66 USB_EN# >>> _____

16,36 USB_OC0# >>> _____

USB Power Switch



USB Power Sharing



3.1 阻值範圍: $\geq 1\Omega$ & 0Ω									
型別	標記 代號	最高 工作電壓	最高 工作電流	T.C.R. (ppm/°C)	阻值 公差	溫度 係數	溫度 係數 公差	JUMPER DCI 阻值	JUMPER DCI 公差
					Block (%) R ₂₅ (%)	Temp (ppm/°C)	Temp (ppm/°C)	1 T ₂₅	2 T ₂₅
RTT01 (020)	1-W 20	25V	50V	± 500 +500 -500	$\pm 10\%$ 10R $\pm 10\Omega$	10R $\pm 10\Omega$	10R $\pm 10\Omega$	0.5A	50mΩ
RTT02 (0402)	1-W 100	50V	100V	± 100 +100 -100	100R $\pm 10\%$ 100R $\pm 10\Omega$	100R $\pm 22\%$	100R $\pm 22\%$	1A	50mΩ
RTT03 (0603)	1-W 75V	150V		± 100 +100 -100	100R $\pm 10\%$ 100R $\pm 10\Omega$	100R $\pm 22\%$	100R $\pm 22\%$	1A	50mΩ
RTT05 (0805)	1-W 80V	150V	300V	± 100 +100 -100	100R $\pm 10\%$ 100R $\pm 10\Omega$	100R $\pm 22\%$	100R $\pm 22\%$	2A	50mΩ

USB2.0 from USB Charger

```

36 USB3_CHAR_N <<>>-----
36 USB3_CHAR_P <<>>-----

```

USB3.1

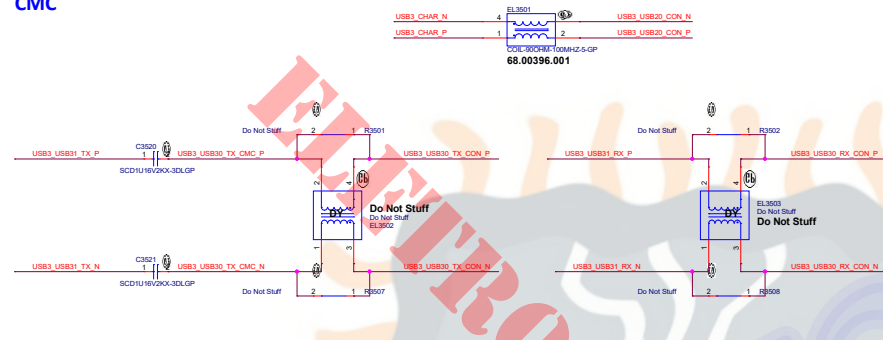
```

16 USB3_USB31_TX_P  >>>
16 USB3_USB31_TX_N  >>>

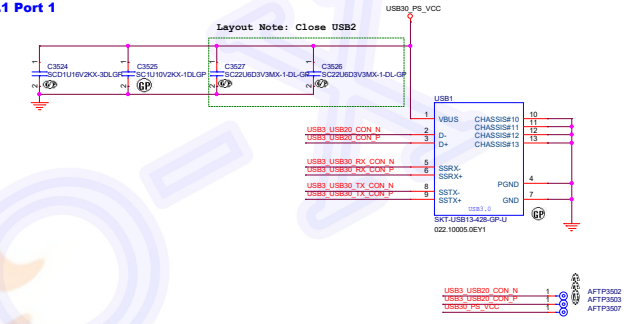
16 USB3_USB31_RX_P  <<<
16 USB3_USB31_RX_N  <<<

```

CMC



USB-A Connector
USB3.1 Port 1



USB2.0

16 USB4_USB20_N <<>>

16 USB4_USB20_P <<>>

USB3.1

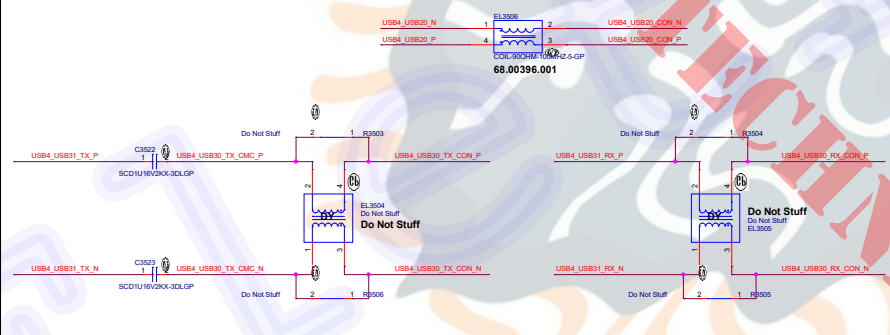
```

16 USB4_USB31_TX_P  >>>
16 USB4_USB31_TX_N  >>>

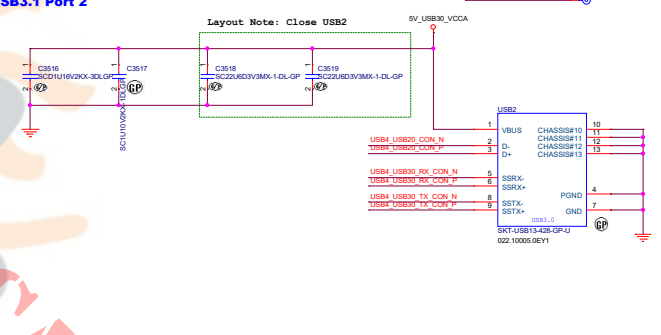
16 USB4_USB31_RX_P  <<<
16 USB4_USB31_RX_N  <<<

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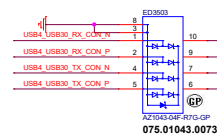
CMC



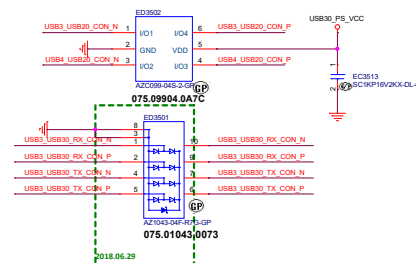
USB-A Connector
USB3.1 Port 2



ESD FOR PORT1



ESD FOR PORT2



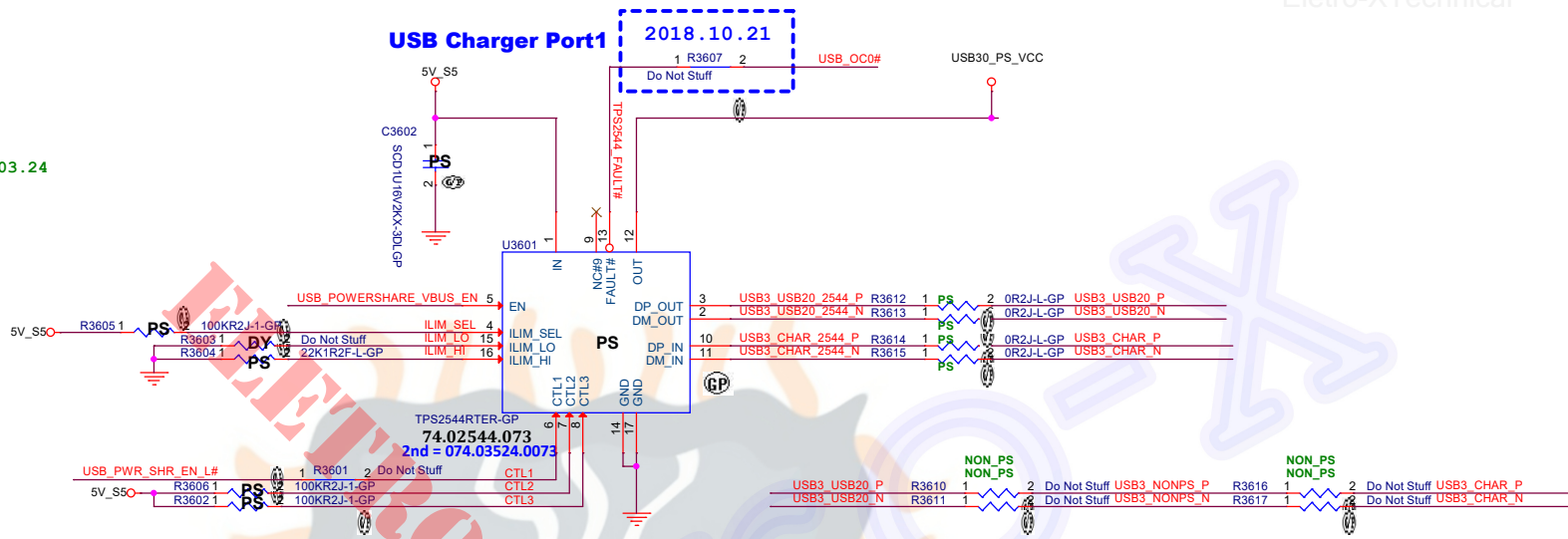
Main Func = USB Charger

Eletro-XTechnical

2018.03.24

USB Charger Port1

2018.10.21



- 35 USB3_CHAR_P <<<>>>
- 35 USB3_CHAR_N <<<>>>
- 16 USB3_USB20_P <<<>>>
- 16 USB3_USB20_N <<<>>>
- 24 USB_POWERSHARE_VBUS_EN >>>
- 24 USB_PWR_SHR_EN_L# >>>
- 16,35 USB_OC0# <<<


Device Control Pins				
	CTL1 (EC control)	CTL2	CTL3	ILIM_SEL
CDP	1	1	1	1
DCP Auto	0	1	1	X

The following equation programs the typical current limit:

$$I_{OS_vp} (mA) = \frac{50,500}{(R_{ILIM_XX} (k\Omega) + 0.1)}$$

R_{ILIM,XX} corresponds to either R_{ILIM,HI} or R_{ILIM,LO} as appropriate.

BOLT L 0823



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB Charger

Rev

A00

Size

Custom

Document Number

BOLT WHL

Date:

Thursday, December 27, 2018

Sheet

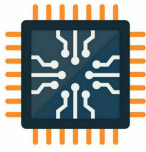
36

of

105

Eletro-XTechnical

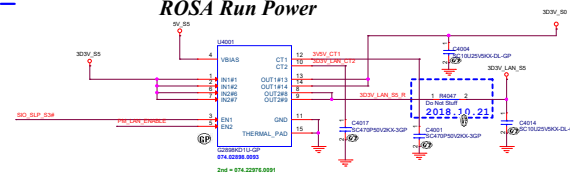
Eletro-XTechnical



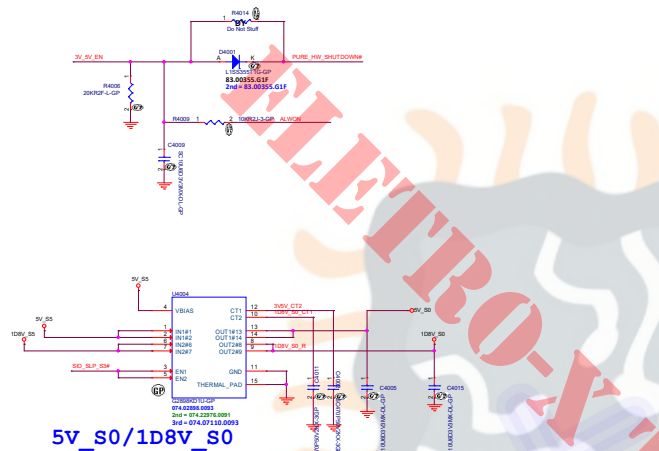


3D3V_S0/5V_S0

ROSA Run Power



3D3V_S0/LAN POWER



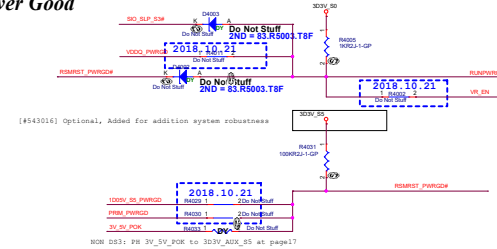
5V_S0/1D8V_S0

Table 4. Rise Time Values

CT (pF)	5 V	3.3 V	1.8 V	1.5 V	1.2 V	1.05 V	0.6 V
0	149	112	77	70	60	56	42
220	548	388	236	206	173	154	103
470	968	673	401	342	289	256	169
1000	1768	1220	711	608	505	445	286
2200	3916	2678	1554	1332	1097	949	627
4700	8040	5477	3179	2691	2240	1964	1249
10000	16520	11150	6410	5401	4430	3933	2526

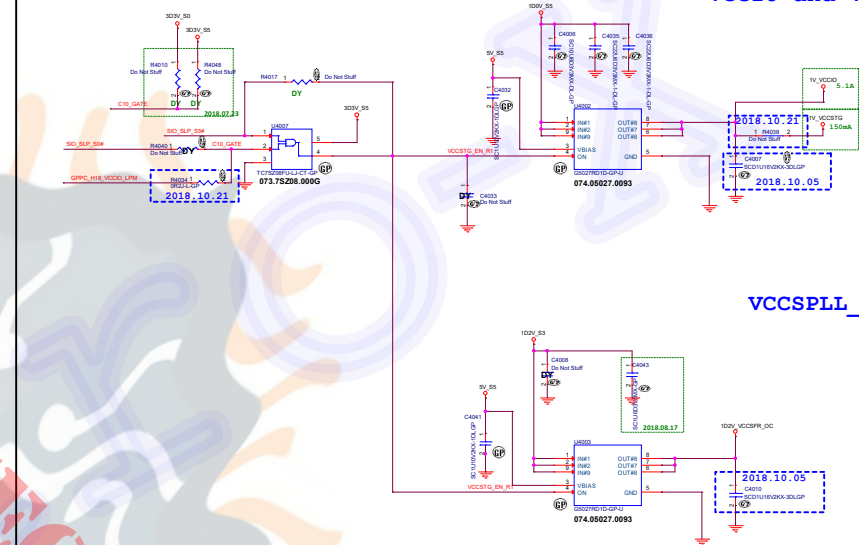
(1) TYPICAL VALUES at 25°C, V_{BIAS} = 5 V, 25 V X7R 10% CERAMIC CAP

Power Good



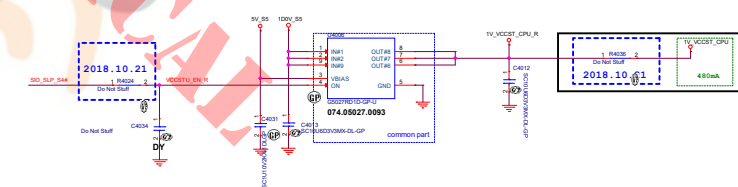
Eletro-XTechnical

VCCIO and VCCSTG



VCCSPLL_OC

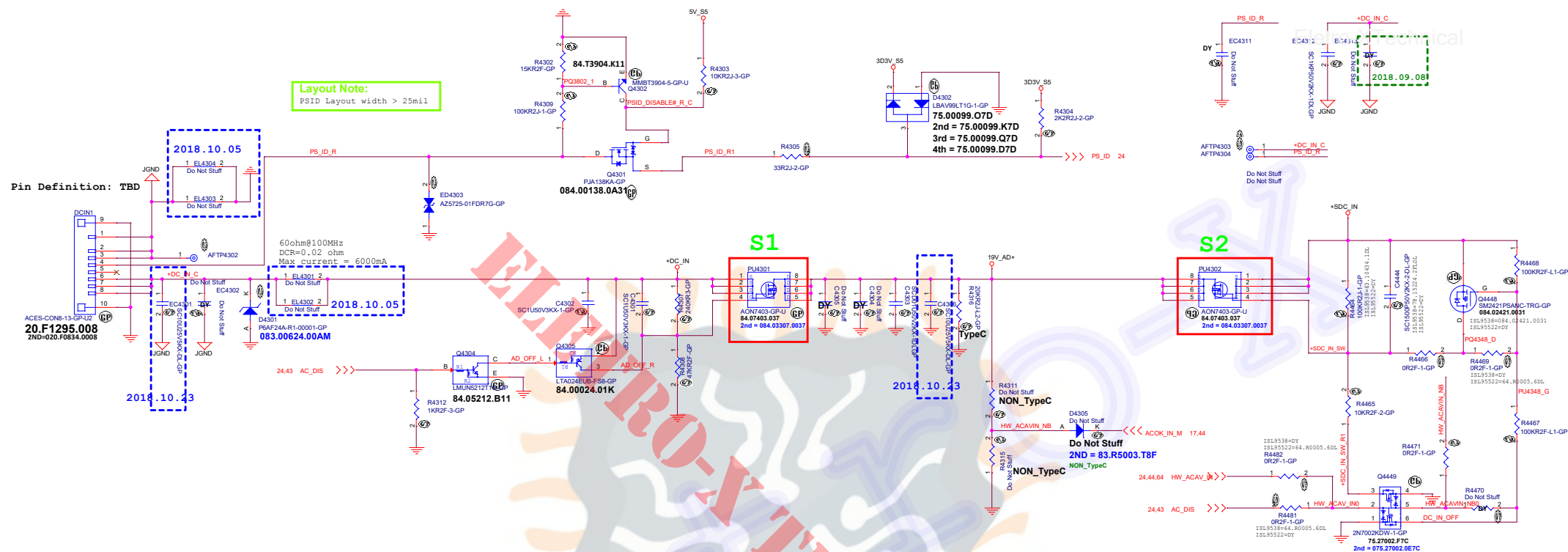
VCCST/VCCPLL



Eletro-XTechnical

Eletro-XTechnical

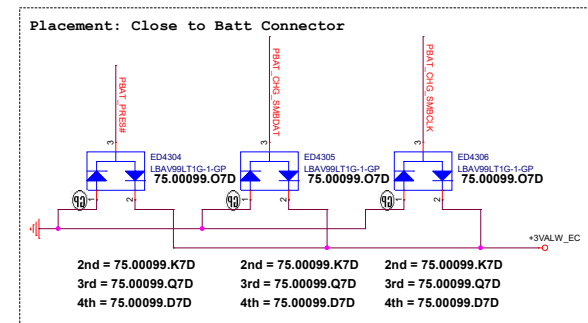
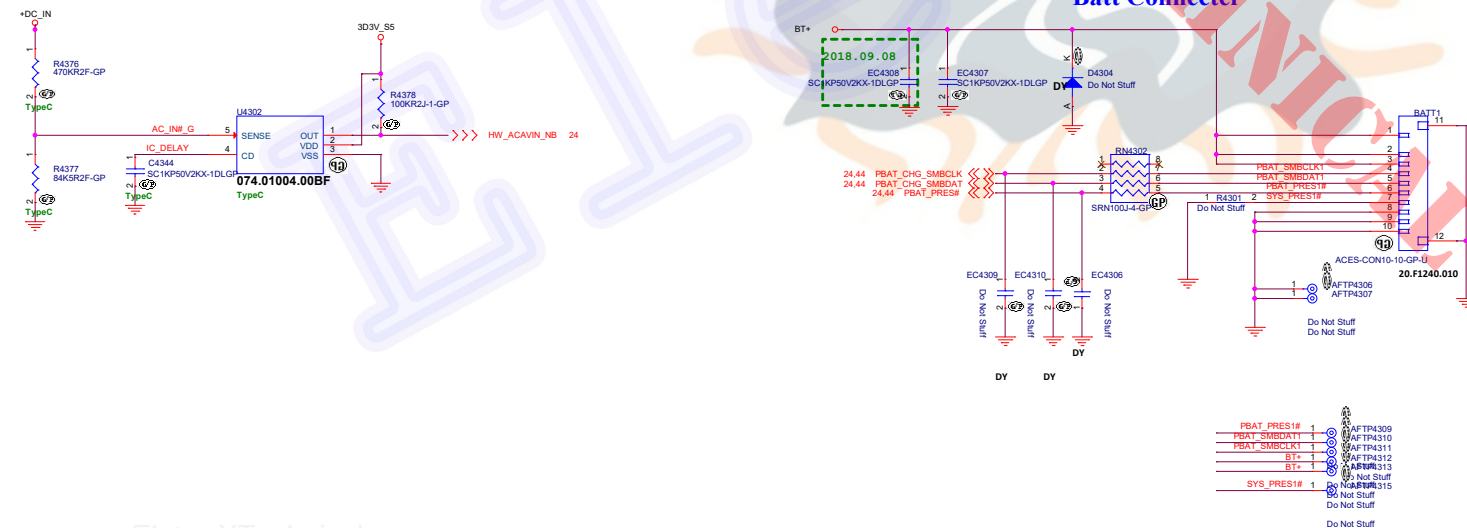
5
Main Func = ADT Input



Main Func = Barrel Adapter Piug-in Detect

Main Func = M-BAT Input

Batt Connector

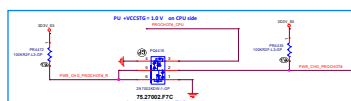
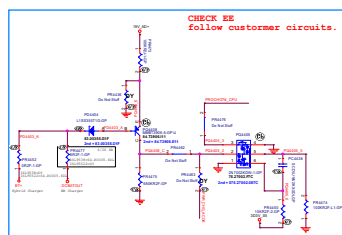
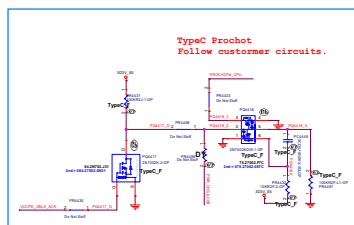
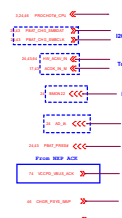


Default

ISL95522 Hybrid Charger

ISL9538 Buck-Boost Charger

OFF PAGE



BOM Change List

Year	Country	Year	Country	Year	Country	Year	Country
1990	AD	1990	AD	1990	AD	1990	AD
1991	AE	1991	AE	1991	AE	1991	AE
1992	AF	1992	AF	1992	AF	1992	AF
1993	AG	1993	AG	1993	AG	1993	AG
1994	AI	1994	AI	1994	AI	1994	AI
1995	AL	1995	AL	1995	AL	1995	AL
1996	AM	1996	AM	1996	AM	1996	AM
1997	AO	1997	AO	1997	AO	1997	AO
1998	AR	1998	AR	1998	AR	1998	AR
1999	AS	1999	AS	1999	AS	1999	AS
2000	AT	2000	AT	2000	AT	2000	AT
2001	AU	2001	AU	2001	AU	2001	AU
2002	AW	2002	AW	2002	AW	2002	AW
2003	AX	2003	AX	2003	AX	2003	AX
2004	BA	2004	BA	2004	BA	2004	BA
2005	BB	2005	BB	2005	BB	2005	BB
2006	BD	2006	BD	2006	BD	2006	BD
2007	BE	2007	BE	2007	BE	2007	BE
2008	BF	2008	BF	2008	BF	2008	BF
2009	BG	2009	BG	2009	BG	2009	BG
2010	BH	2010	BH	2010	BH	2010	BH
2011	BI	2011	BI	2011	BI	2011	BI
2012	BJ	2012	BJ	2012	BJ	2012	BJ
2013	BK	2013	BK	2013	BK	2013	BK
2014	BL	2014	BL	2014	BL	2014	BL
2015	BM	2015	BM	2015	BM	2015	BM
2016	BN	2016	BN	2016	BN	2016	BN
2017	BO	2017	BO	2017	BO	2017	BO
2018	BR	2018	BR	2018	BR	2018	BR
2019	BS	2019	BS	2019	BS	2019	BS
2020	BT	2020	BT	2020	BT	2020	BT
2021	BV	2021	BV	2021	BV	2021	BV
2022	BW	2022	BW	2022	BW	2022	BW
2023	BY	2023	BY	2023	BY	2023	BY
2024	BZ	2024	BZ	2024	BZ	2024	BZ
2025	CA	2025	CA	2025	CA	2025	CA
2026	CC	2026	CC	2026	CC	2026	CC
2027	CD	2027	CD	2027	CD	2027	CD
2028	CE	2028	CE	2028	CE	2028	CE
2029	CF	2029	CF	2029	CF	2029	CF
2030	CG	2030	CG	2030	CG	2030	CG
2031	CH	2031	CH	2031	CH	2031	CH
2032	CI	2032	CI	2032	CI	2032	CI
2033	CK	2033	CK	2033	CK	2033	CK
2034	CL	2034	CL	2034	CL	2034	CL
2035	CM	2035	CM	2035	CM	2035	CM
2036	CN	2036	CN	2036	CN	2036	CN
2037	CO	2037	CO	2037	CO	2037	CO
2038	CR	2038	CR	2038	CR	2038	CR
2039	CU	2039	CU	2039	CU	2039	CU
2040	CV	2040	CV	2040	CV	2040	CV
2041	CW	2041	CW	2041	CW	2041	CW
2042	CX	2042	CX	2042	CX	2042	CX
2043	CY	2043	CY	2043	CY	2043	CY
2044	CZ	2044	CZ	2044	CZ	2044	CZ
2045	DA	2045	DA	2045	DA	2045	DA
2046	DB	2046	DB	2046	DB	2046	DB
2047	DD	2047	DD	2047	DD	2047	DD
2048	DE	2048	DE	2048	DE	2048	DE
2049	DF	2049	DF	2049	DF	2049	DF
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2051	DH	2051	DH	2051	DH	2051	DH

ISL9538

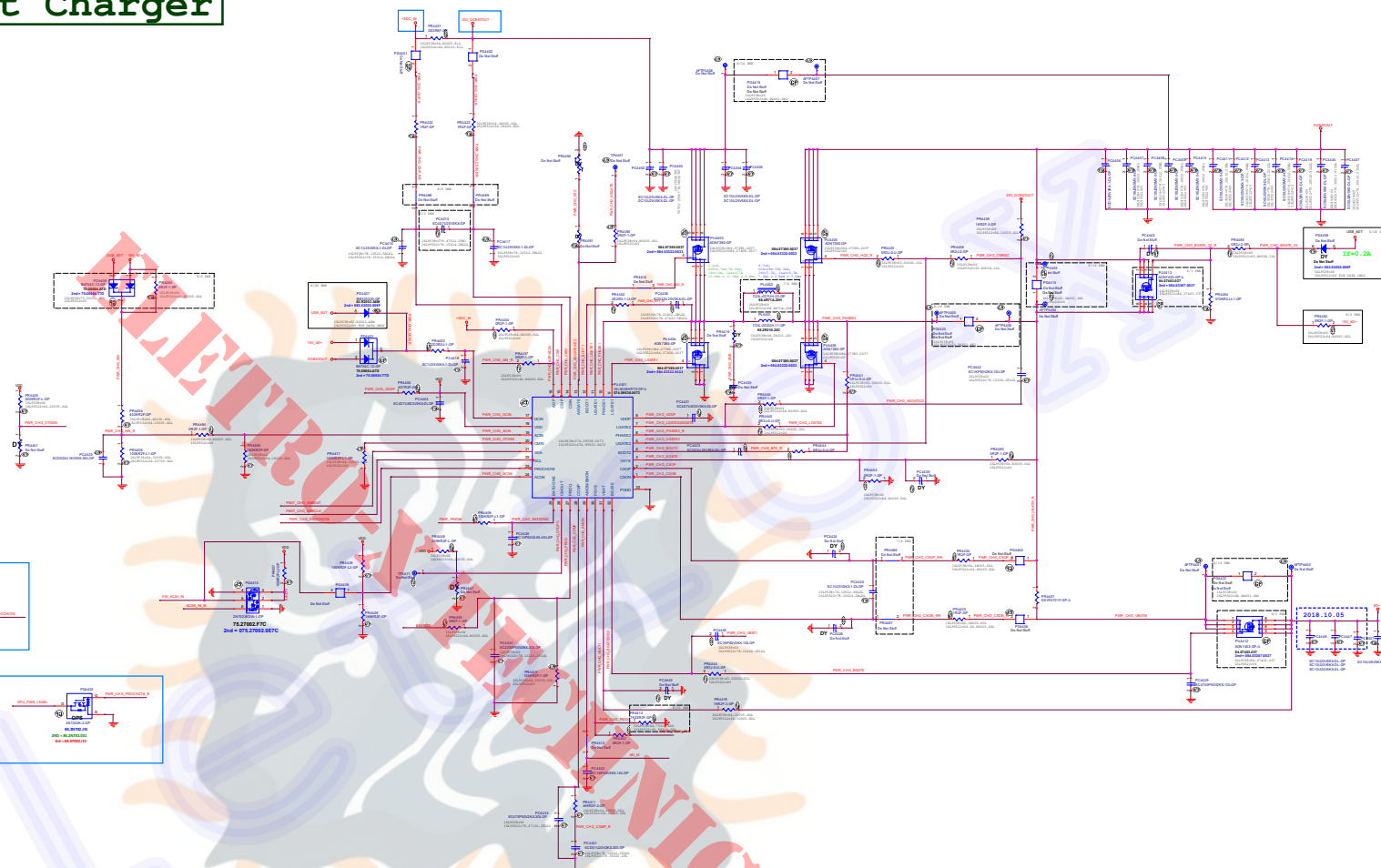
TABLE 22. PROG PIN PROGRAMMING OPTIONS

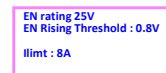
[illegible]

ISL95522

Table 17. Prog Pin Programming Options

Table 17. Ping-Pong Configuration Options			
Prog/GND Resistance (kΩ)	Charger Type	Current Sense Resistor Value	Default # of Battery Cells in Series
Typ (1% Standard Resistor)	0	NVDC	
22.8		$R_{CS} = R_{CS} + 2$ $R_{CS} = 3m\Omega$	3
38.3		$R_{CS} = 3m\Omega$	4
		$R_{CS} = 25m\Omega$ $R_{CS} = 3m\Omega$	2
69.6		$R_{CS} = R_{CS} + 1$ $R_{CS} = 3m\Omega$ $R_{CS} = 10m\Omega$	3
86.6		$R_{CS} = 10m\Omega$	4
102		$R_{CS} = 25m\Omega$	2
150		$R_{CS} = 25m\Omega$ $R_{CS} = 25m\Omega$	2
182			3
215		$R_{CS} = R_{CS} + 2$ $R_{CS} = 10m\Omega$ $R_{CS} = 3m\Omega$	4
237		$R_{CS} = 3m\Omega$	3
255		$R_{CS} = 25m\Omega$	2
	1	FBP	
		$R_{CS} = R_{CS} + 1$ $R_{CS} = 10m\Omega$ $R_{CS} = 3m\Omega$	4
		$R_{CS} = 3m\Omega$	3
		$R_{CS} = 25m\Omega$	2

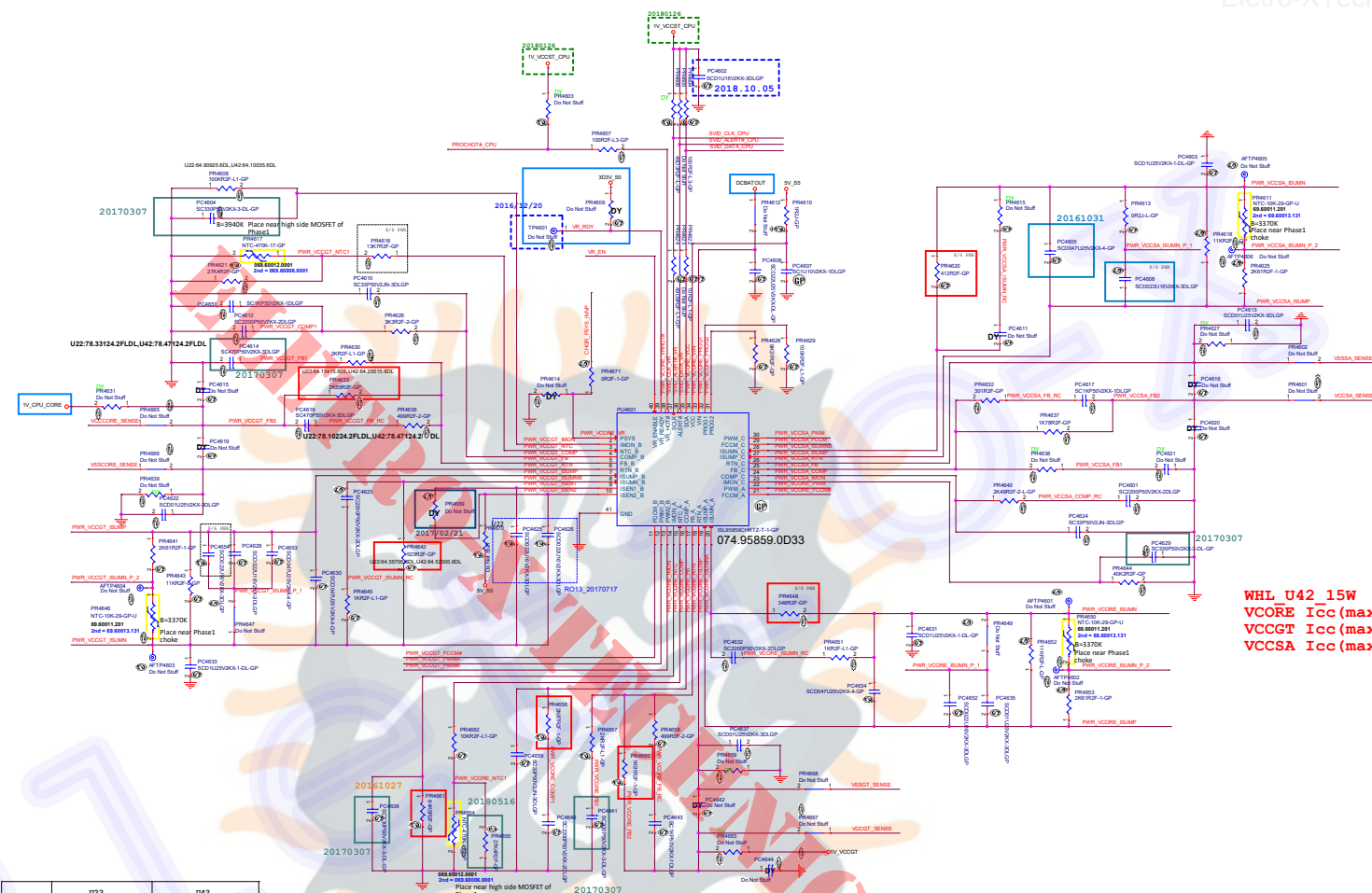




$I_{cc}(\max) = 7A$
 $I_{cc} = 4.7A$
 $OCP > 8A$



BOLT L 0823



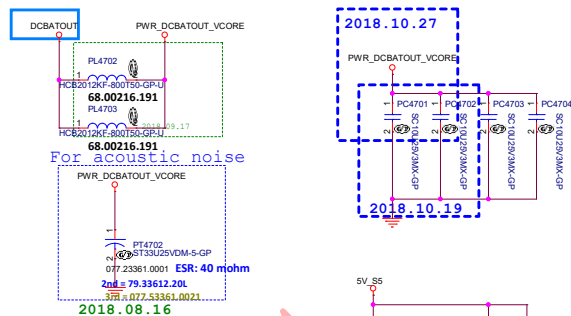
WHL U42_15W
 VCCORE Icc(max)=70A TDC=48 A
 VCCCT Icc(max)=31A TDC=18 A
 VCCSA Icc(max)=6A TDC=4A

	U22	U42	
PC4614	330p (78.33124.2FLDL)	470p (78.47124.2FLDL)	
PC4618	1Kp (78.10224.2FLDL)	470p (78.47124.2FLDL)	2017/04/25
PC4625	DY	0.022u (78.22321.2FLDL)	
PC4626	DY	0.022u (78.22321.2FLDL)	
PC4669		DY	2017/02/21
PR4670	1K (64.10015.6DL)	DY	
PR4642	357 (64.35705.6DL)	523 (64.52305.6DL)	2018/04/27
PC4630	47nF (078.47322.02PD)	47nF (078.47322.02PD)	
PC4628	22nF (78.22321.2FLDL)	22nF (78.22321.2FLDL)	
PC4654	22nF (78.22321.2FLDL)	22nF (78.22321.2FLDL)	2018/08/06
PC4653	DY	47nF (078.47322.02PD)	
PR4633	1.54K (64.15415.6DL)	2.55K (64.25515.6DL)	
PR4608	90.9K (64.90925.6DL)	100K (64.10035.6DL)	2018/04/27

Main FUNC = CPU CORE

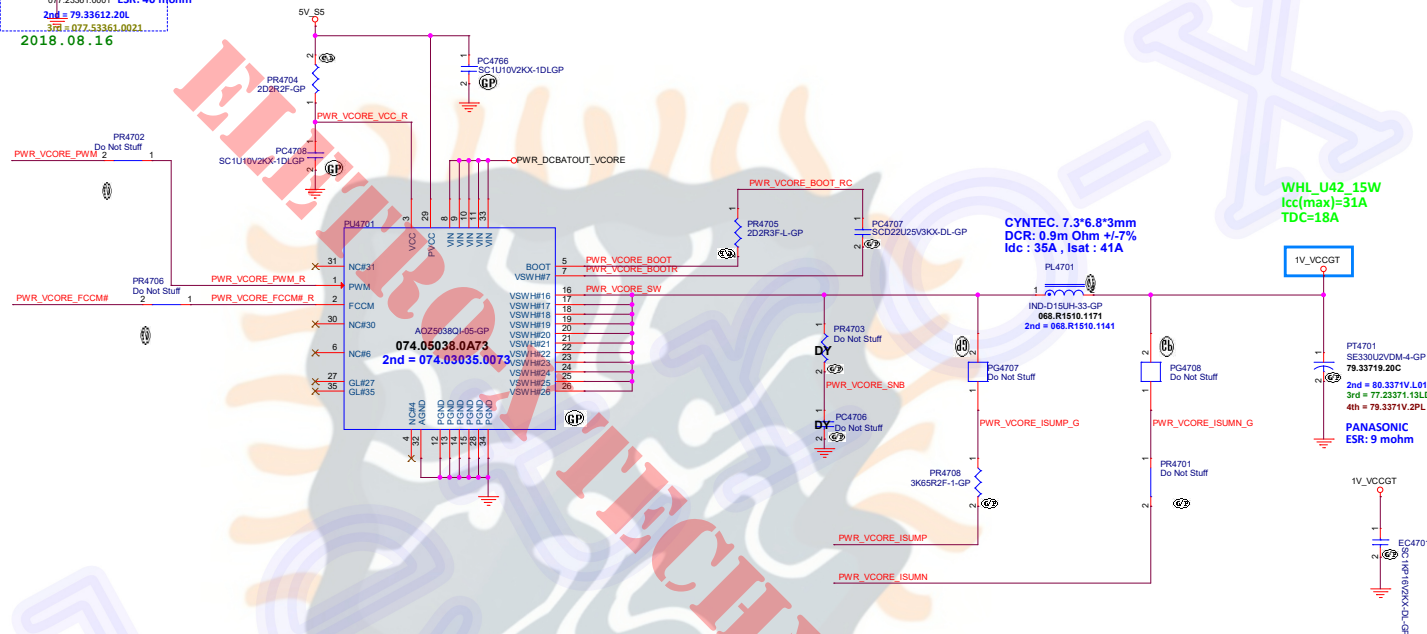
2018.09.17

46 PWR_VCORE_PWM
46 PWR_VCORE_FCCM#
46 PWR_VCORE_ISUMP
46 PWR_VCORE_ISUMN



For acoustic noise

2018.08.16



Eletro-XTechnical

WHL_U42_15W
Icc(max)=31A
TDC=18A

CYNTEC 7.3*6.8*3mm
DCR: 0.9m Ohm +/-7%
I_{dc}: 35A, I_{sat}: 41A

PANASONIC
ESR: 9 mohm

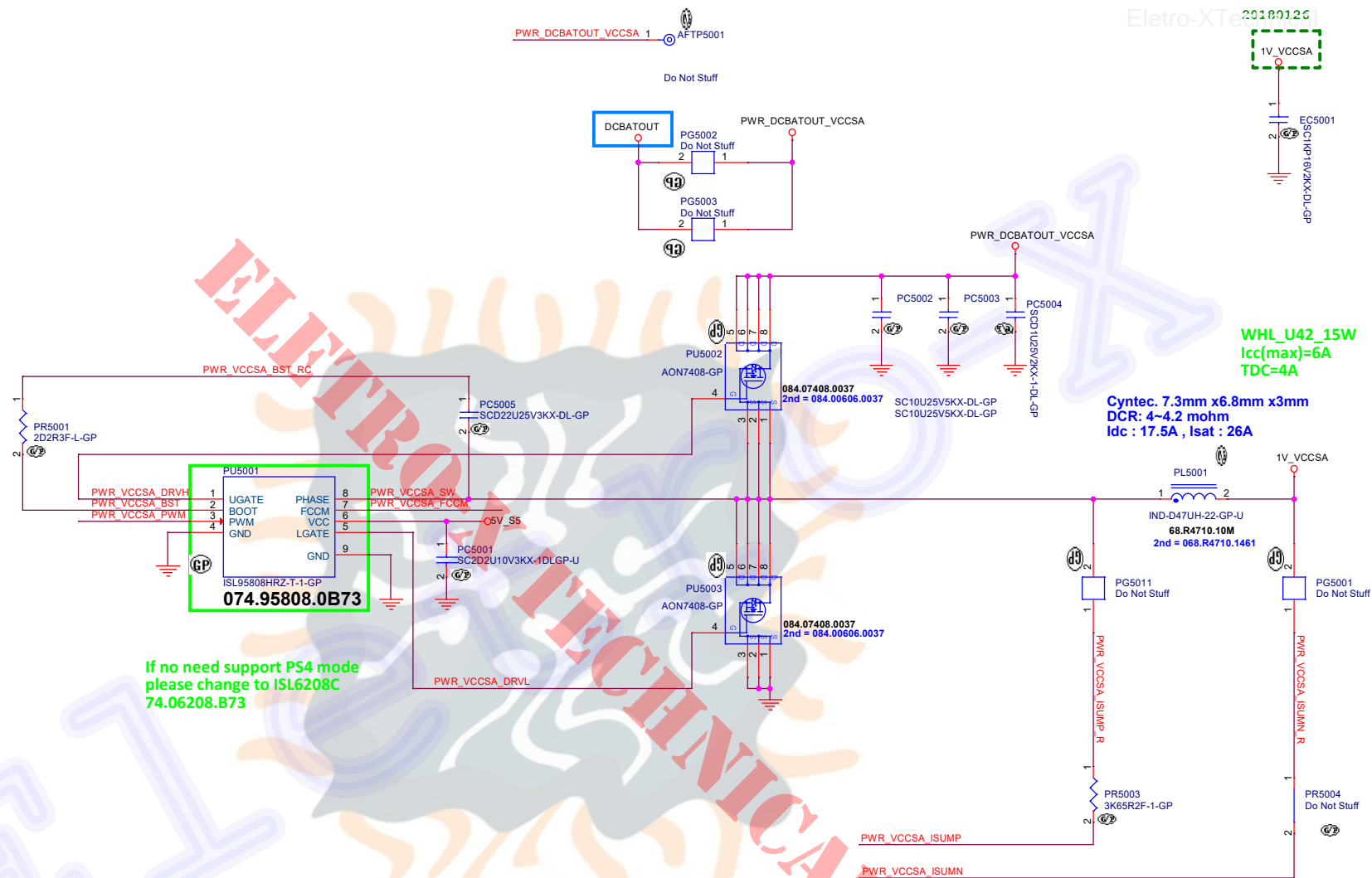
1V_VCCGT

PT4701
SE330U2VDM-4-GP
79.33719.20C
2nd = 80.3371V.L01
3rd = 77.23371V.L01
4th = 79.3371V.2PL

BOLT L 0823



Main FUNC = CPU CORE



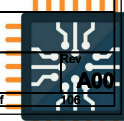
If no need support PS4 mode
please change to ISL6208C
74.06208.B73

BOLT L 0823

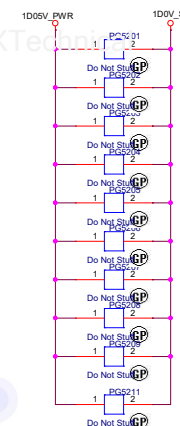


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
VCCSA Technical			
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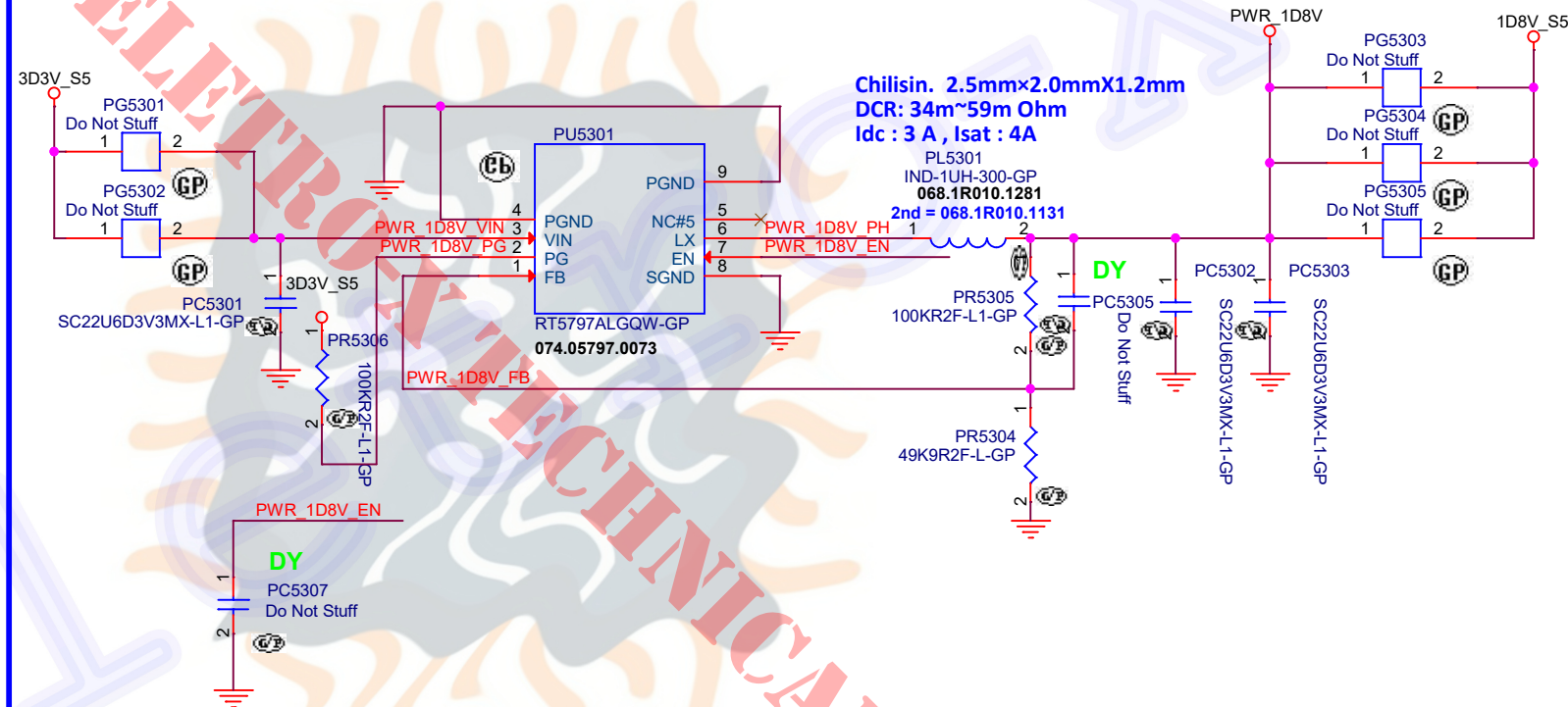


Main Func = 1D8V

Eletro-XTechnical

Icc(max)=0.902A
Icc=0.632A
OCP>3A

52 PWR_1D8V_PC <<< _____
25 3V_5V_DSW_OK >>> 2 PR5308 1 PWR_1D8V_EN
Do Not Stuff
2018.10.21



BOLT L 0823



Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

1D8V

Size
A4

Document Number

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Date: Thursday, December 27, 2018

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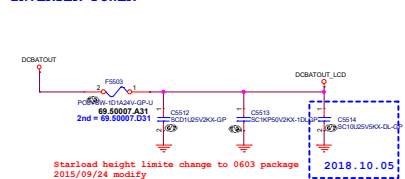


Eletro-XTechnical

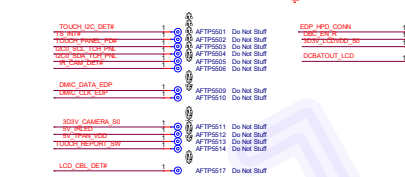
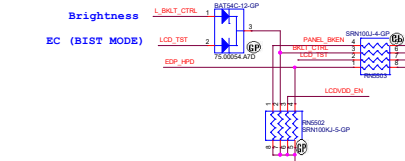
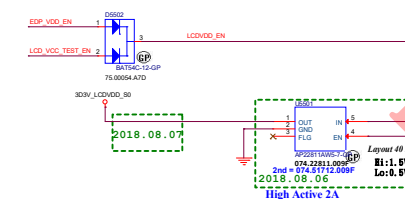
Eletro-X

Main Func = LCD

INVERTER POWER



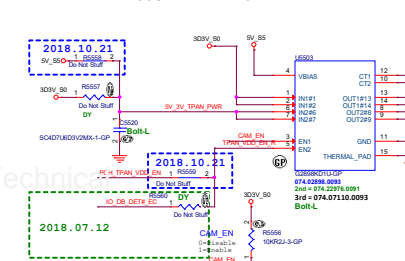
LCDVDD



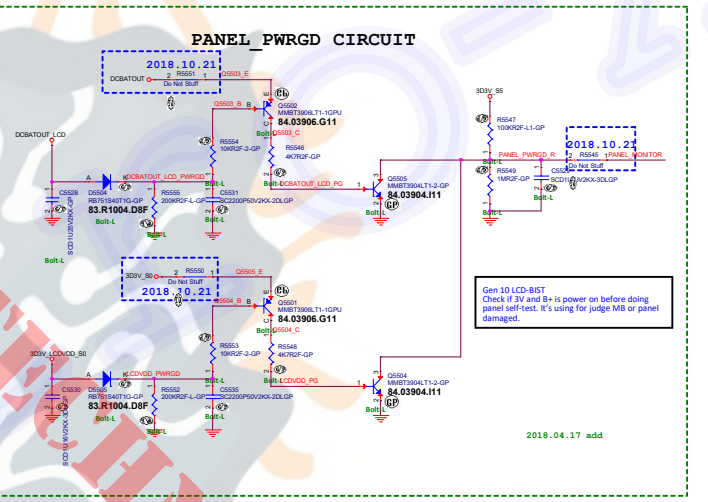
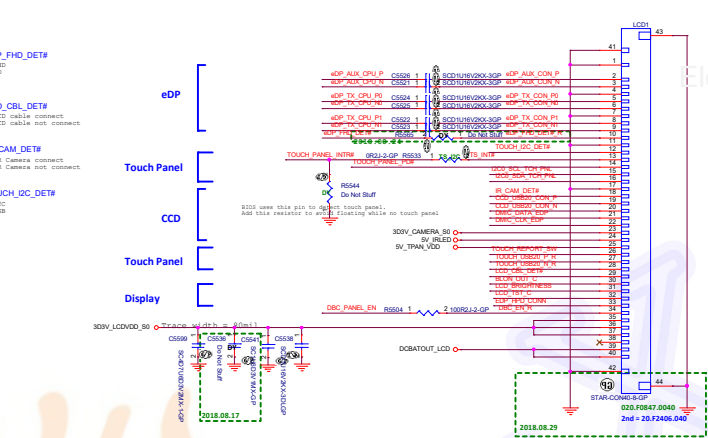
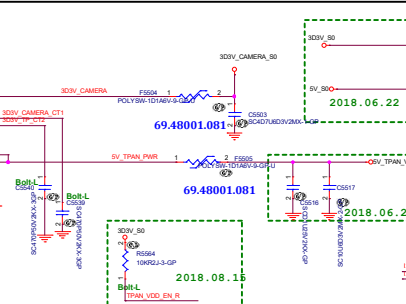
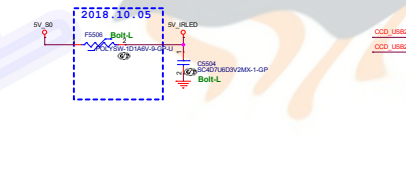
Main Func = CAMERA



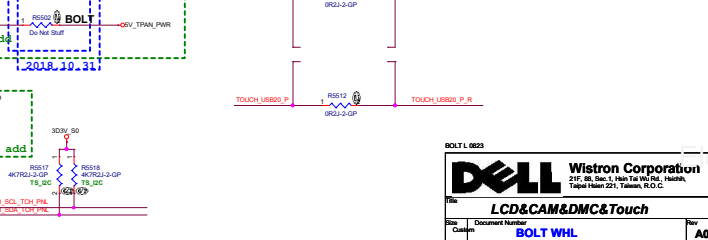
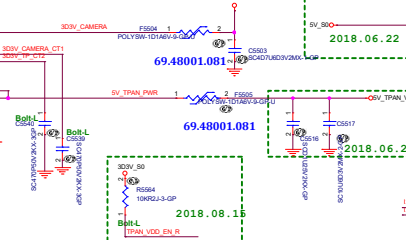
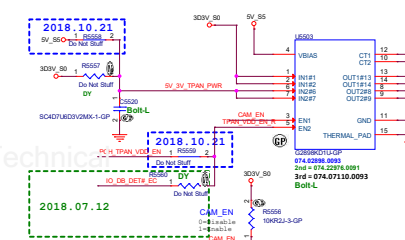
TOUCH PANEL POWER



IR LED POWER

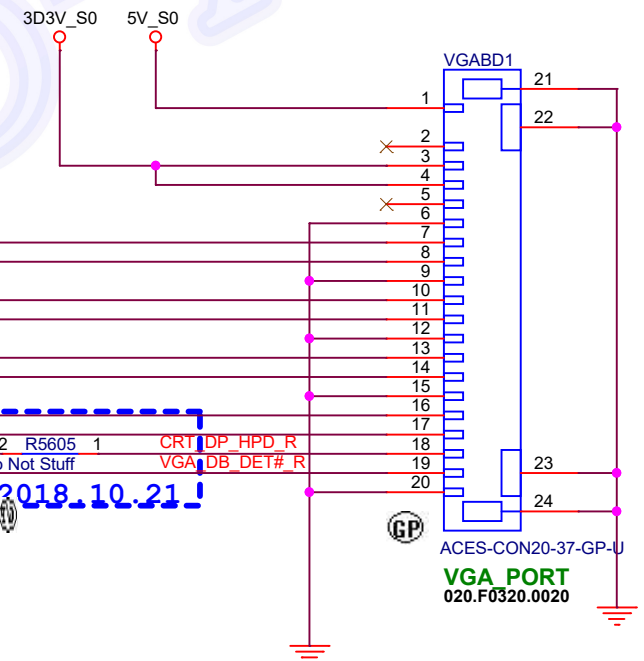
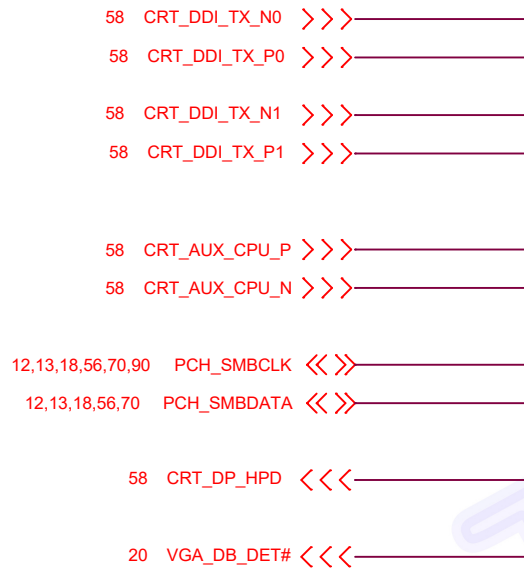


Main Func = Touch panel



Main Func = CRT

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BOLT L 0823

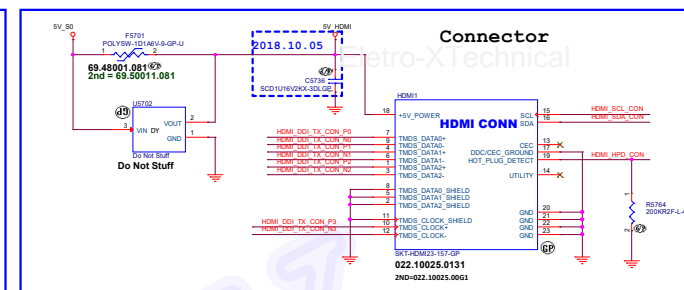
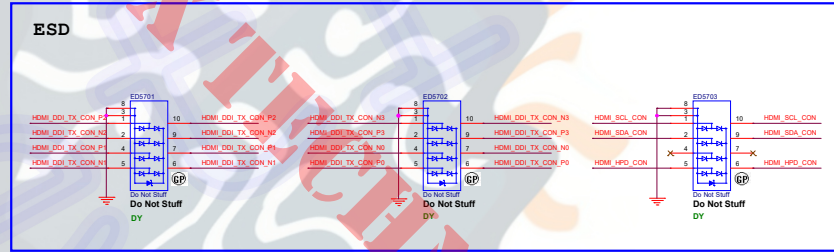
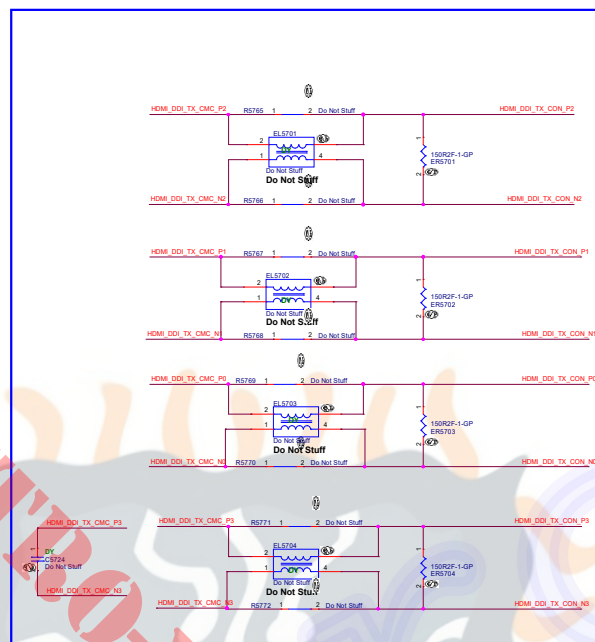
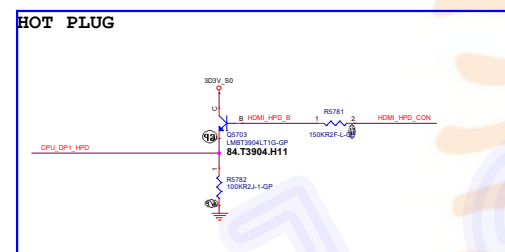
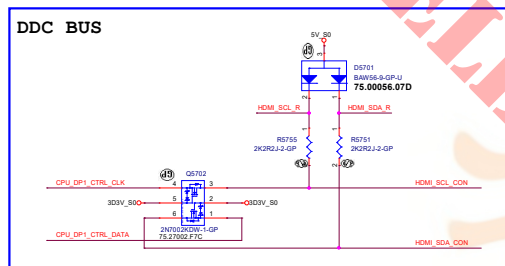
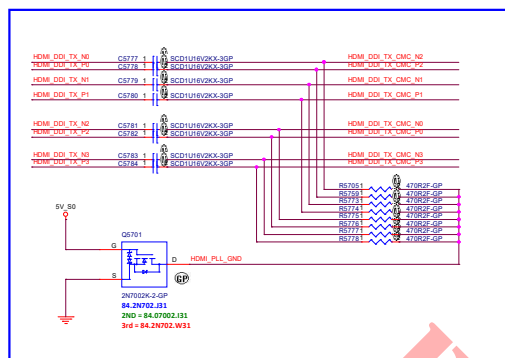


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Taipei Hsien 221, Taiwan, R.O.C.

Title		CRT	
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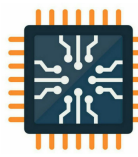
4 HDMI_DDI_TX_N0 >>>
 4 HDMI_DDI_TX_P0 >>>
 4 HDMI_DDI_TX_N1 >>>
 4 HDMI_DDI_TX_P1 >>>
 4 HDMI_DDI_TX_N2 >>>
 4 HDMI_DDI_TX_P2 >>>
 4 HDMI_DDI_TX_N3 >>>
 4 HDMI_DDI_TX_P3 >>>
 4 CPU_DP1_HPD <<<

4.88 CPU_DP1_CTRL_CLK <<<
 4 CPU_DP1_CTRL_DATA <<<



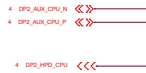
BOLT.1.0023

DELL		Wistron Corporation	
HDMI		21F, 3B, 5C, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100	
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Customer	BOLT WHL		
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Main Func = DP Demux

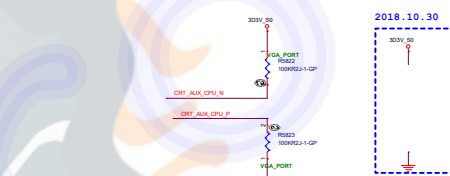
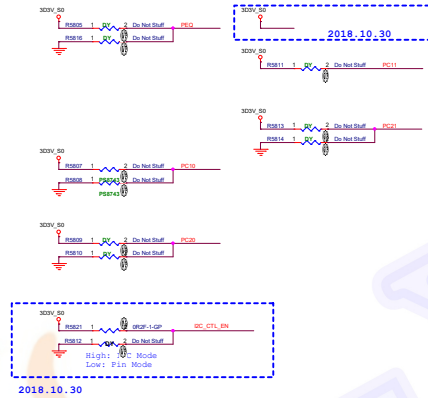
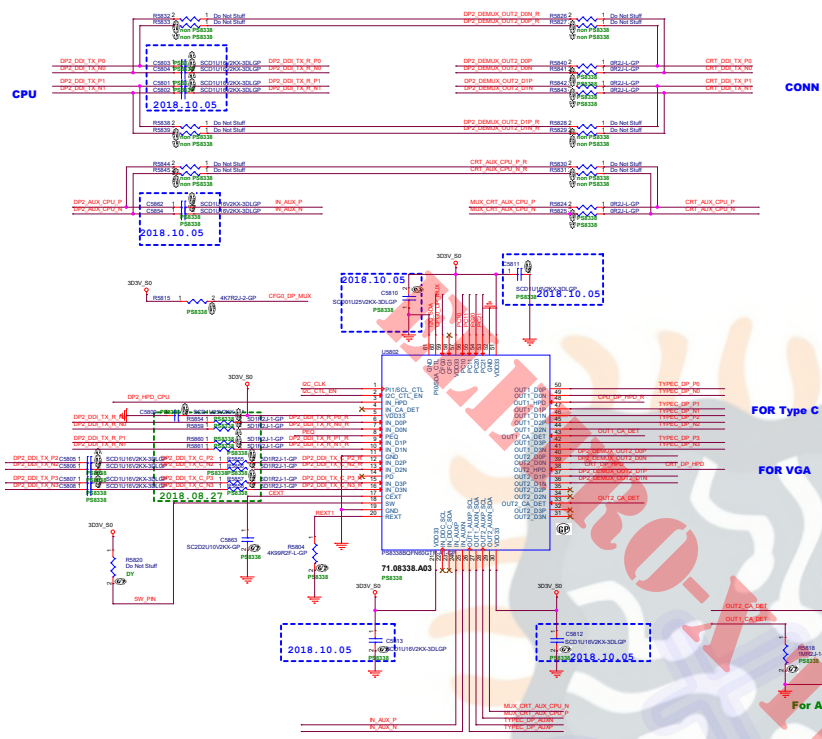
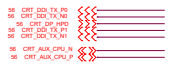
CPU DP to DP De-MUX



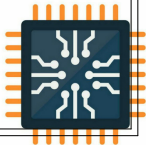
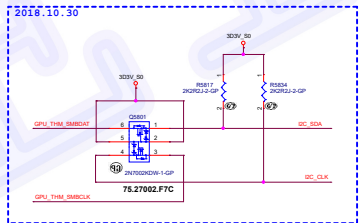
FOR Type C



FOR VGA



SW	I/O	<p>Port switching control or priority configuration. Internal pull down ~150KΩ, 3.3V I/O</p> <p>For Control Switching Mode (CFG0 = L):</p> <p>SW = L: Port1 is selected (default)</p> <p>SW = H: Port2 is selected</p> <p>For Automatic Switching Mode (CFG0 = H):</p> <p>SW = L: Port1 has higher priority when both ports are plugged (default)</p> <p>SW = H: Port2 has higher priority when both ports are plugged</p> <p>Overwritten by I2C register in I2C Control Mode</p>
----	-----	--

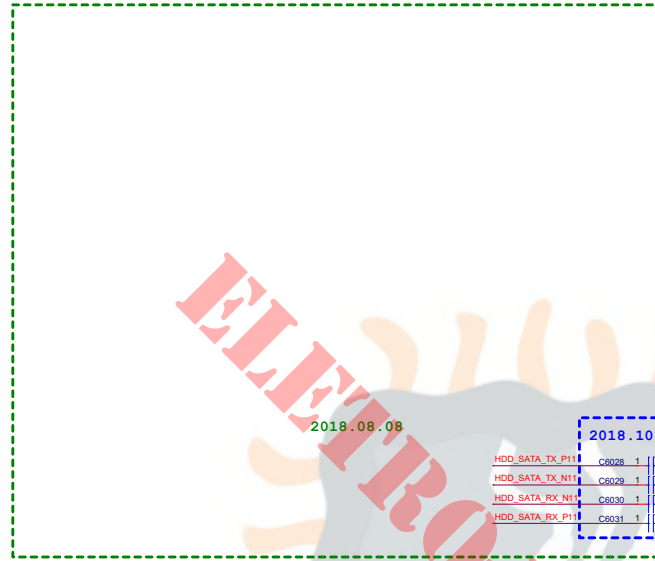


Main Func = HDD

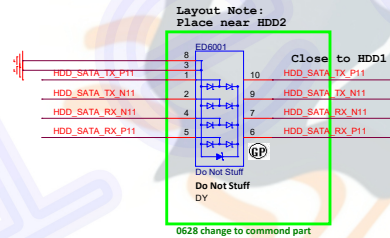
HDD



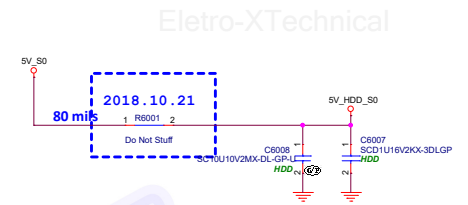
SATA RE-DRIVER



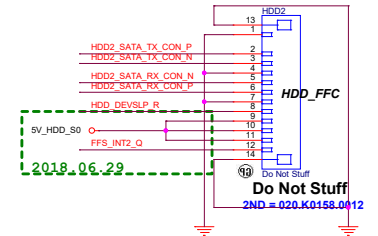
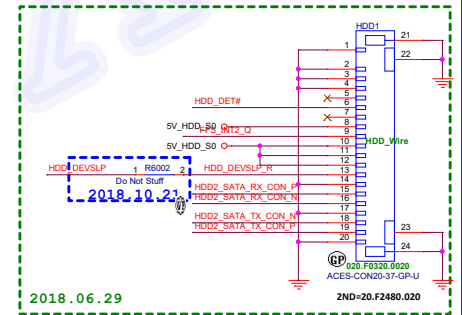
HDD ESD



HDD POWER

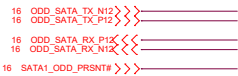


SATA HDD Connector

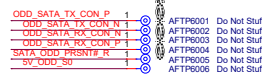
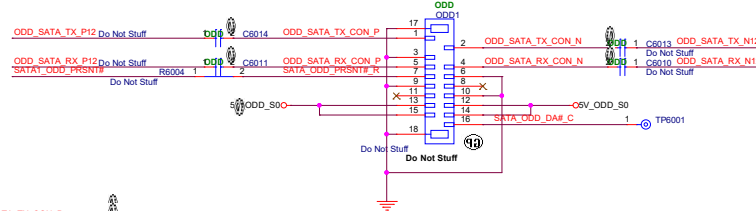
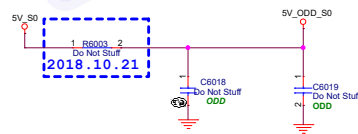


Main Func = ODD

ODD



ODD Connector



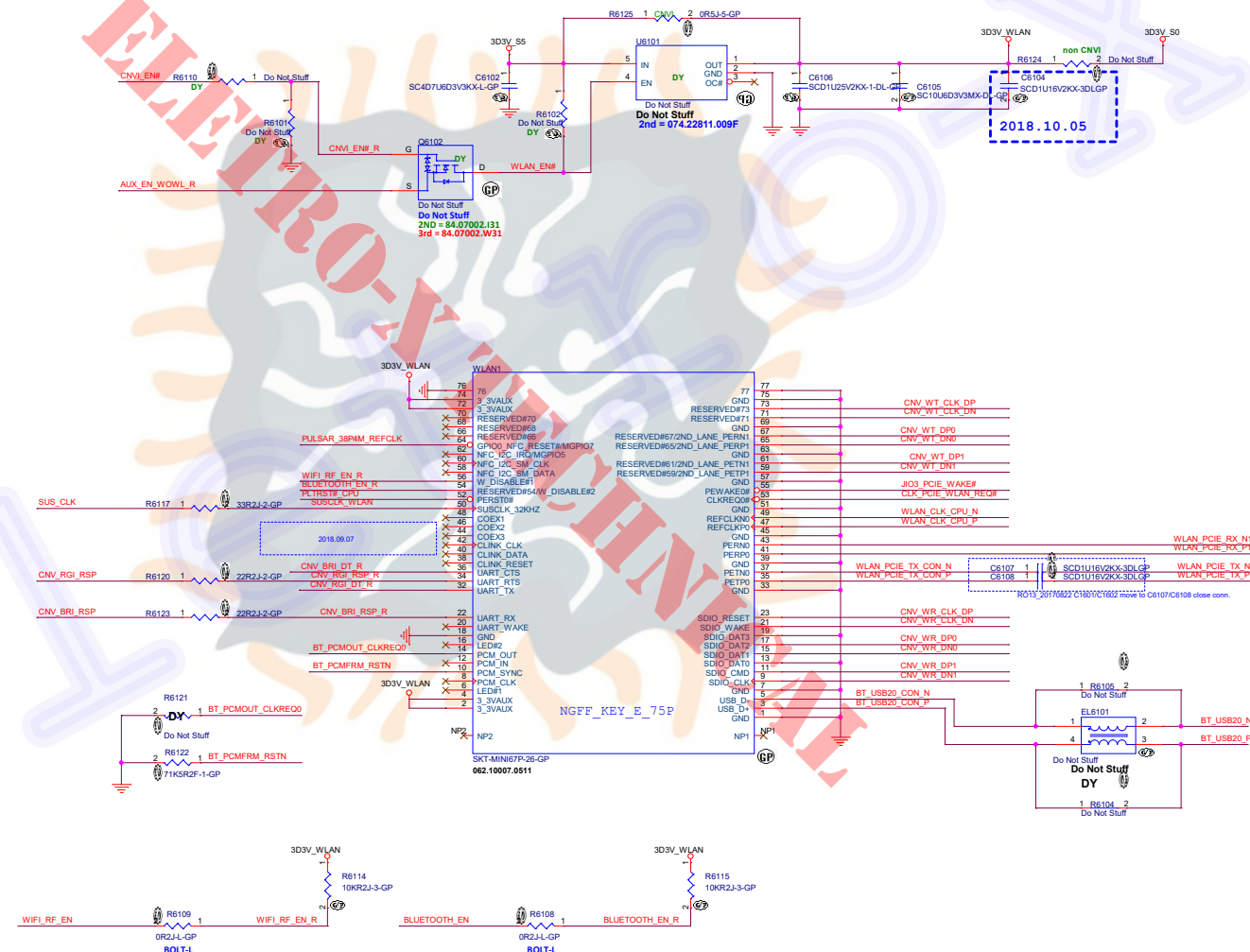
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WLAN

CNVI

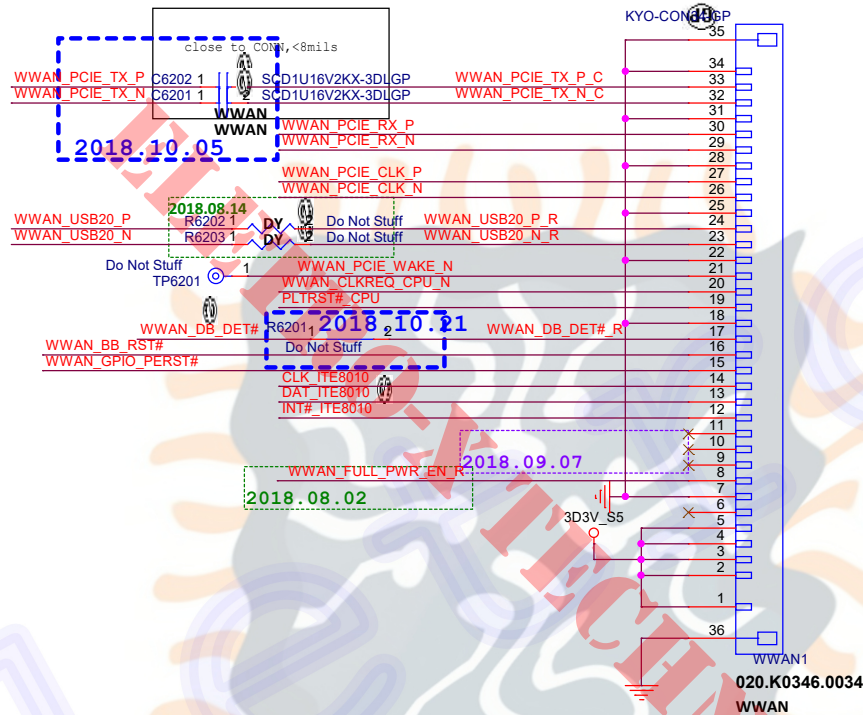
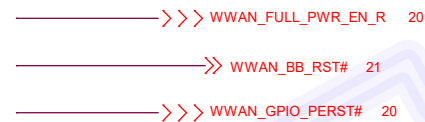
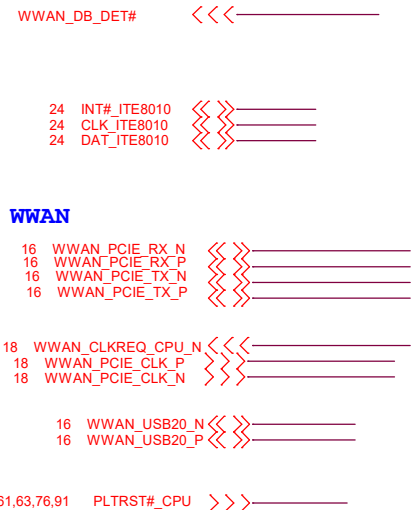
Others

CPU		WLAN
GPP_F8_RXD	COEX1	UART TXD
GPP_F9_TXD	COEX2	UART RXD
GPP_F0_BLANKING	COEX3	STANDARD PIN



Main FUNC = WWAN

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Title

WWAN

Size

Document Number

Custom

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2018.08.02

[illegible]

SSD M.2 CONN

PCIE:1 SATA:0

2018.08.07

Important! SATA Host DEVSLP signals shall not be terminated since device shall terminate the signal.

- This is an open-drain pin on the PCH side. PCH will tri-state this pin to signal to SATA device that it may enter a lower power state (pin will go high due to pull-up that's internal to the SATA device, per DEVSLP specification). PCH will drive pin to signal an exit from DEVSLP state.
- When used in PCH, no external pull-up or pull-down termination required for SATA Host DEVSLP.

[illegible]

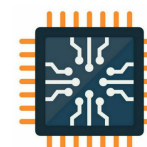
Condition	PCI Express® Gen 2 Only	PCI Express® Gen 3 Only	SATA Only	PCI Express® Gen 2 / SATA	PCI Express® Gen 3 / SATA
Processor Tx	100 nF	220 nF	10 nF ²	100 nF	220 nF
Processor Rx	None	None	10 nF ²	None	None ³

Notes:

- Design Constraint: For PCIe only application, refer to the PCIe guidelines for details.
- Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if COUpled DIOs / devices are NOT used.
- Design Constraint: For PCIe® Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support COUpled DIOs / Devices** as a design constraint. For SATA only configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support COUpled DIOs / Devices** as a design constraint. For guidelines in this section, **this option DOES NOT support Signal Design Guidelines**, along with the Signal Design Guidelines.
- Design Constraint: For PCIe® lane that needs to support either **PCIe® Gen2 devices or PCIe® Gen3 devices**, follow the PCIe® Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel.

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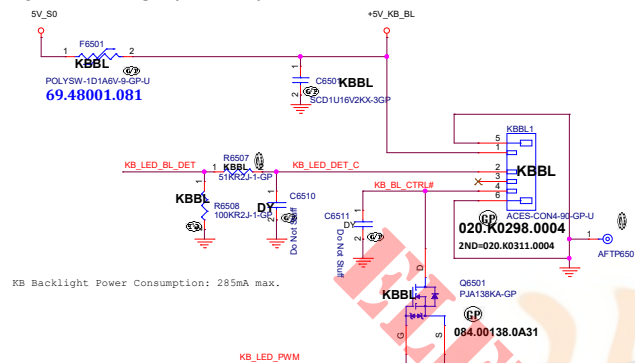
		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
mSATA			
Size	Document Number	Rev A	
Custom	BOLT WHL		
Date	Thursday, December 01 2011	Printed	83 of 106



Main Func = KB

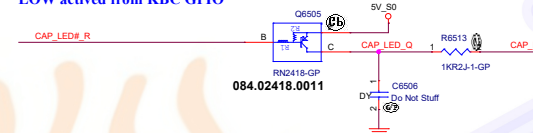
24 CAP_LED#_R >>>
24 KSII[0..7] >>>
24 KSO[0..16] <<<
20 KB_DET# <<<
19 KB_LED_BL_DET <<<
24 KB_LED_PWM >>>

Keyboard Backlight (Reserved)

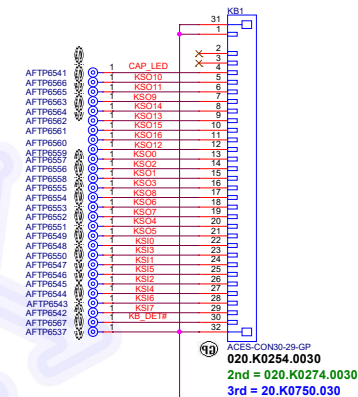


KB Backlight Power Consumption: 285mA max.

CAP LED Control LOW active from KBC GPIO



Internal Keyboard Connector



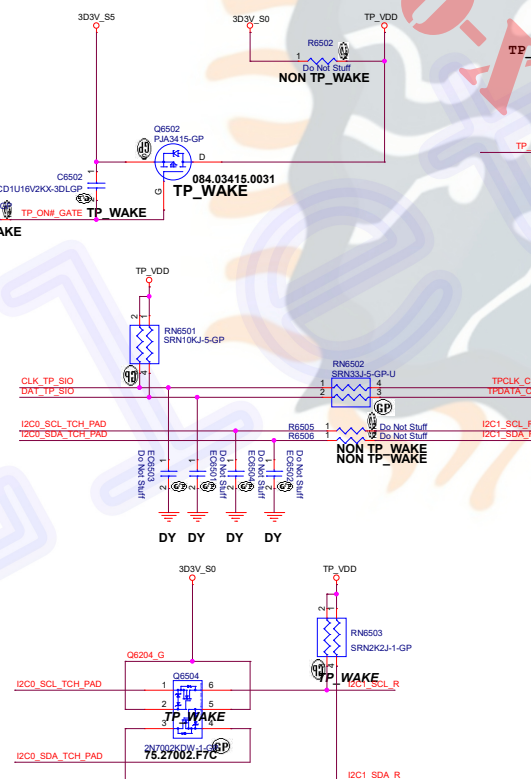
Main Func = TPAD

24 TP_EN# >>>
24 CLK_TP_SIO <<<
24 DAT_TP_SIO <<<
20 I2C0_SCL_TCH_PAD <<<
20 I2C0_SDA_TCH_PAD <<<
3.24 TP_WAKE_KBC# <<<
24 PTP_DIS# >>>

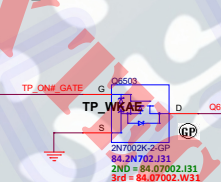
Support PTP

PS2

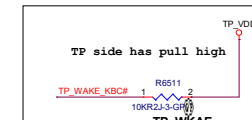
I2C



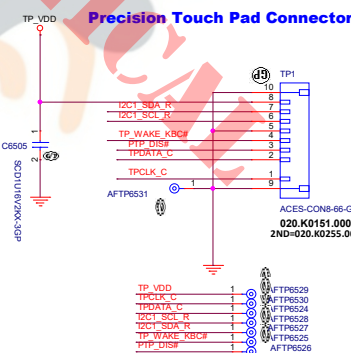
TP_VDD Discharge Circuit



Need to check if it is Active High or Active Low and check if there is PH on TPAD side.



Precision Touch Pad Connector

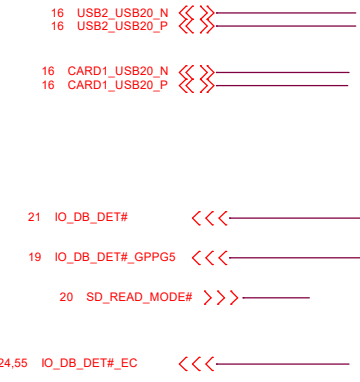


Pin number	Pin name
1	VDD
2	DAT (I2C)
3	CLK (I2C)
4	GND
5	ATTN
6	GPIO
7	DAT (PS2)
8	CLK (PS2)

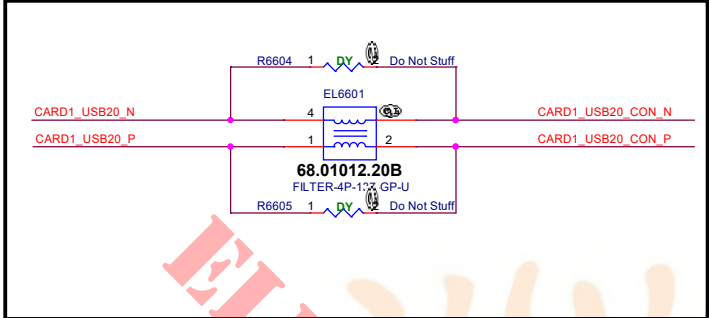
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Main Func = IO Connector

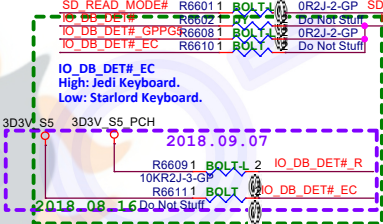
USB 2.0



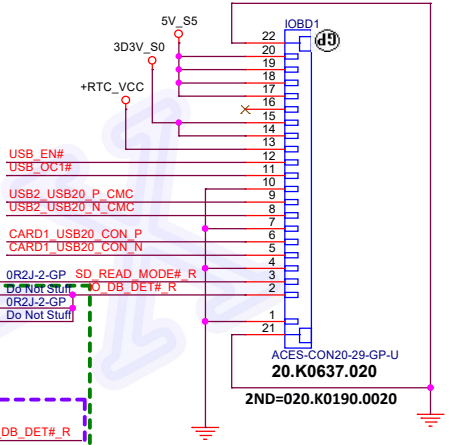
USB2.0 CARD



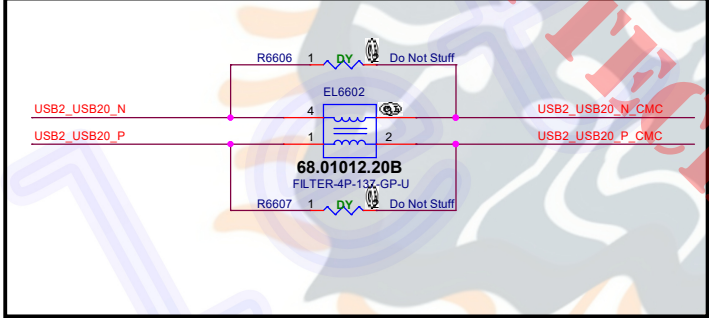
USB2.0
Card Reader SD3.0



Eletro-XTechnical



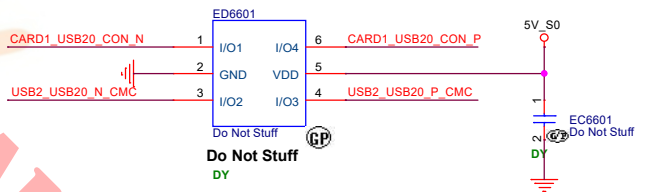
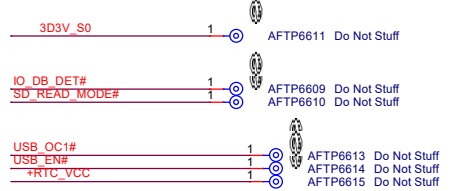
USB2.0 CARD



USB OC



USB Switch Enable



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Title: **IO Board Connector**

Size: Custom Document Number: **BOLT WHL**

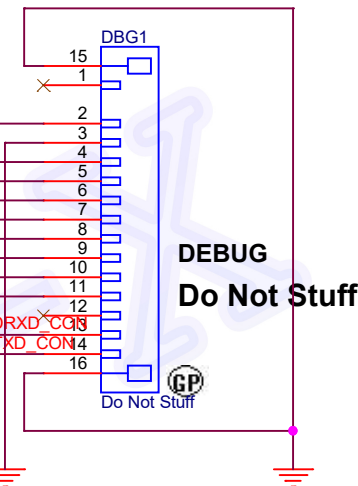
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Eletro-X

Main Func = Debug

Eletro-XTechnical

Debug Connector



18,24 ESPI_CLK
18,24 ESPI_RESET#
18,24 ESPI_CS#

24 HOST_DEBUG_TX

20 UART_2_CTXD_DRXD
20 UART_2_CRXD_DTXD

18,24 ESPI_IO[3..0]

ESPI_IO3
ESPI_IO1
ESPI_IO2
ESPI_IO0

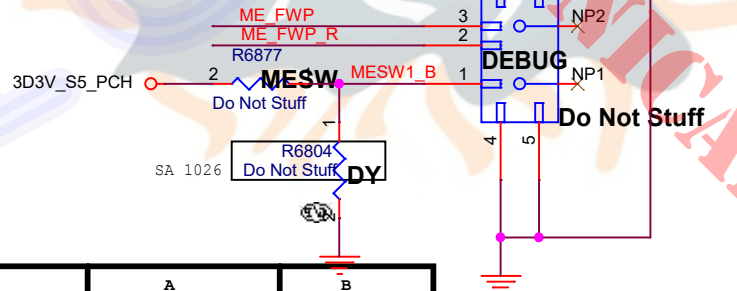
24 ME_FWP

19 ME_FWP_R

Firmware SW

ME_FWP R6878 1 2 0R2J-L-GP ME_FWP_R

NON MESW



	A	B
ME_FWP_R	Low	High
	Normal Operation (Default)	Override

MESW1_B 1 AFTP6801 Do Not Stuff
ME_FWP_R 1 AFTP6802 Do Not Stuff
ME_FWP 1 AFTP6803 Do Not Stuff

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Title

Debug connector

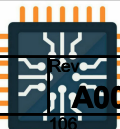
Size
A4

Document Number

BOLT WHL

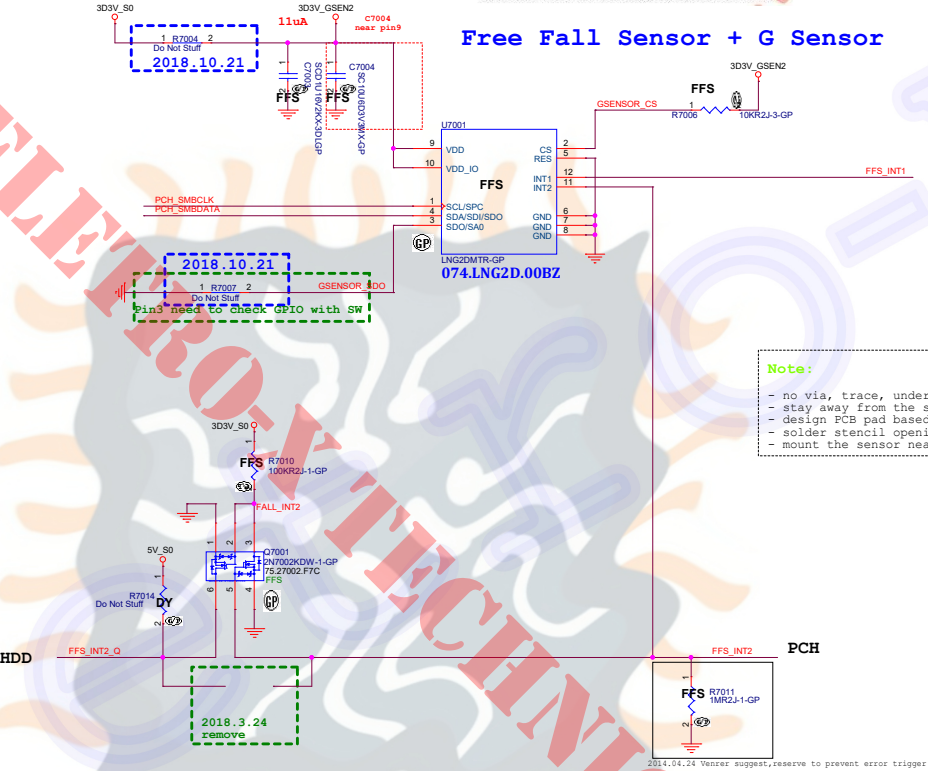
Date: Thursday, December 27, 2018

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The slave address (SAD) associated to the **LNG2DM** is 010100xb. The **SDO/SA0** pad can be used to modify the least significant bit of the device **address**. If the SA0 pad is connected to a voltage supply, LSB is '1' (address 0101001b) or, if the SA0 pad is connected to ground, the LSB value is '0' (address 0101000b). This solution permits two different accelerometers to be connected and addressed to the same I²C lines.

Free Fall Sensor + G Sensor



Note:

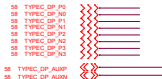
(1) Keep all signals are the same trace width. (included VDD, GND) .

(2) No VIA under IC bottom.

From USB HOST



From DP Demux



From CCG4



From CCG4 to MUX & DP Demux



To Type-C CONNECTOR



USB HOST

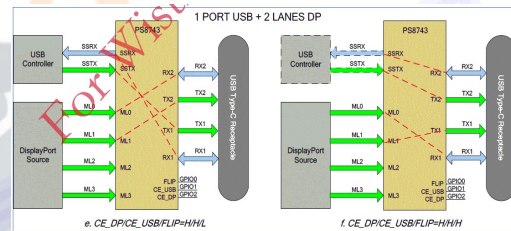
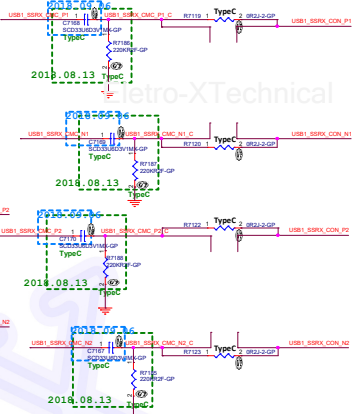
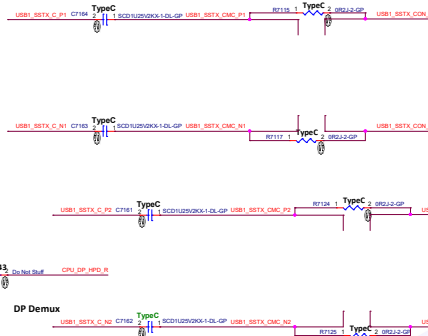
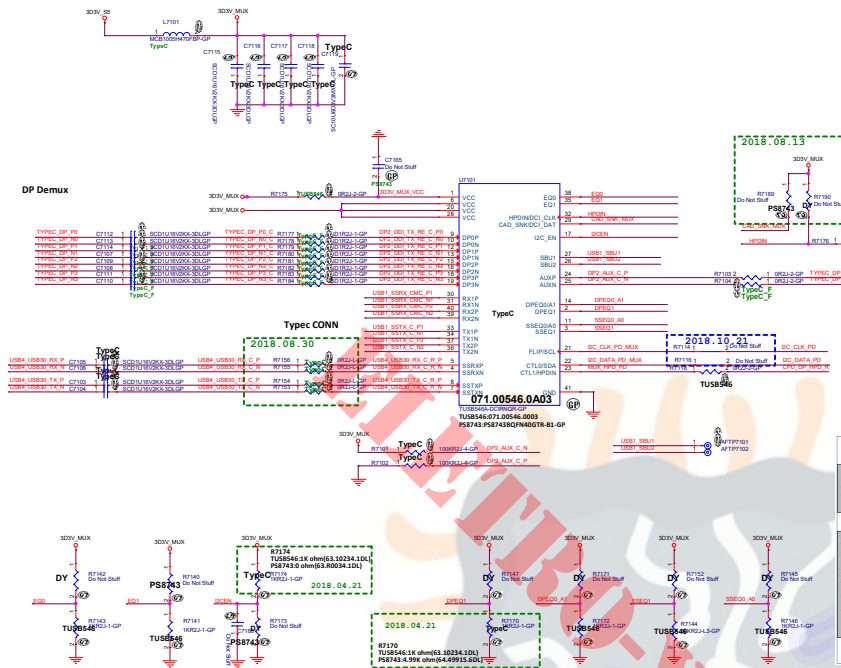
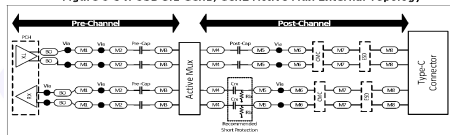


Figure 6-54. USB 3.1 Gen1/Gen2 Active Mux External Topology

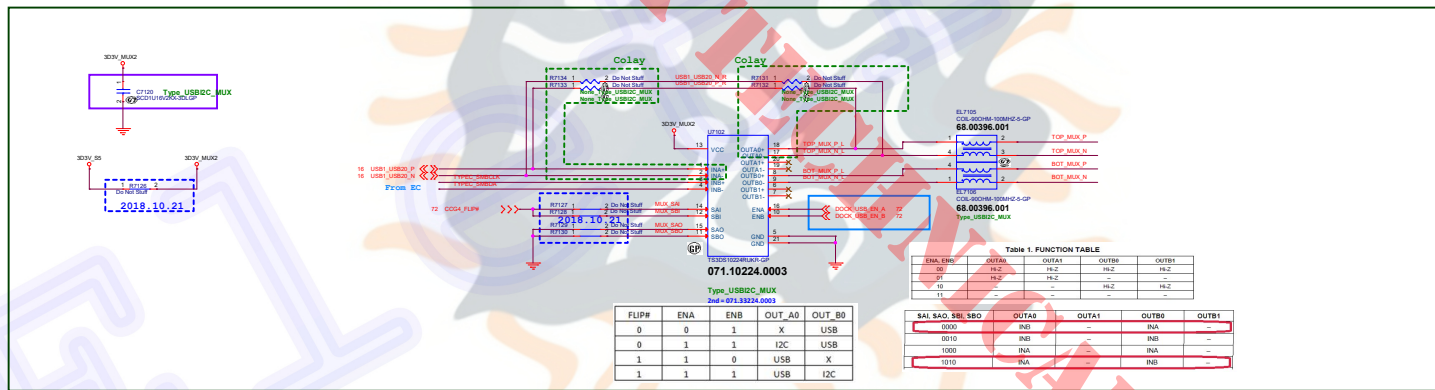
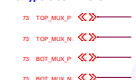


Channel	Parameter	Segment	Stackup	Via Count	Gen2	
					Length (mm)	Length (mils)
Pre-channel	Max Trace Length	B0	MS/SL/DSL	1	Note#1*	Note#1*
	Max Trace Length	M1	MS/SL/DSL	1	Note#1*	Note#1*
	Max Trace Length	M2-M3	M5	0	Note#1*	Note#1*
Post-channel	Max Trace Length	M4 + M5	M5	1	7.6	300
	Max Trace Length	M6-M7	M5		7.6	300
	Max Trace Length	M8	M5		10.2	400

From EC

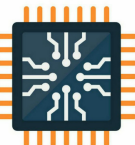
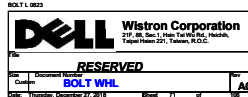


To Type-C CONNECTOR



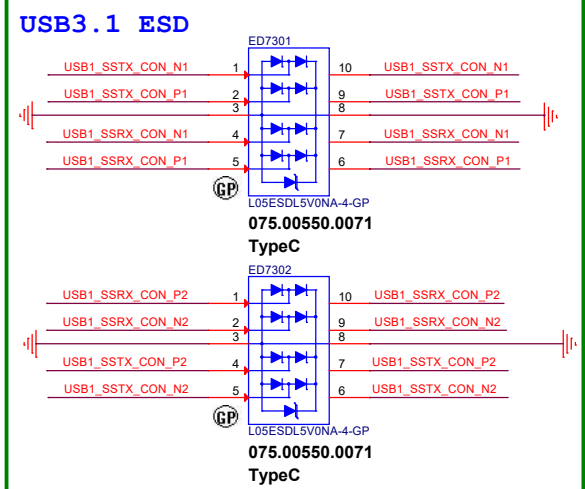
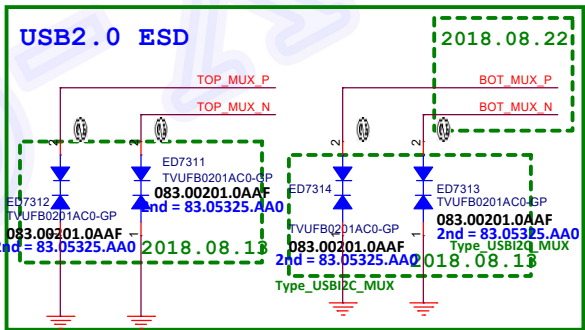
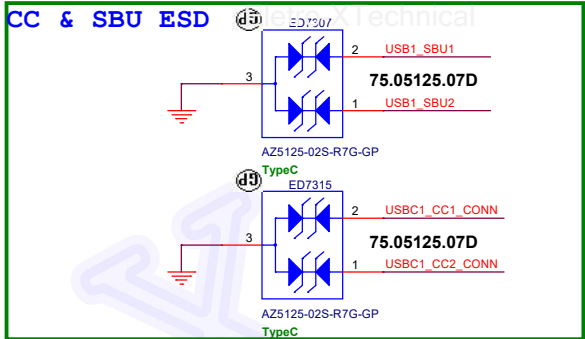
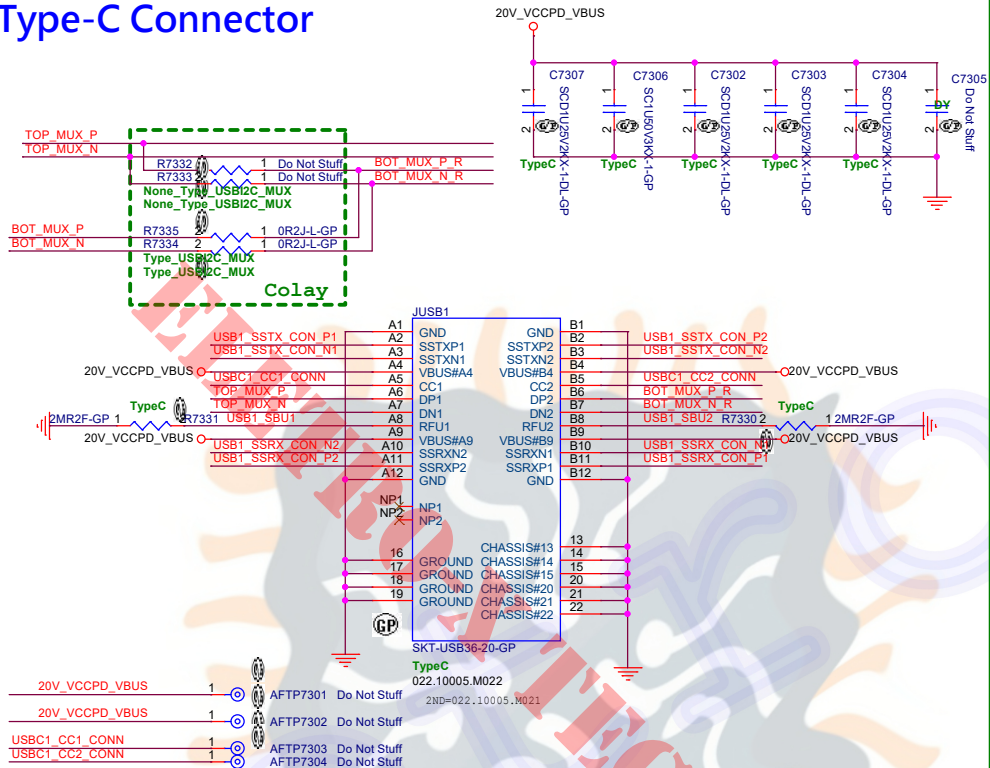
FLIP#	ENA	ENB	OUT_A0	OUT_B0
0	0	1	X	USB
0	1	1	I2C	USB
1	1	0	USB	X
1	1	1	USB	I2C

TOSH 1 FUNCTION TABLE					
ENA	ENB	OUTA0	OUTA1	OUTB0	OUTB1
0000	000	HL2	HL2	HL2	HL2
0010	000	HL2	HL2	HL2	HL2
1000	000	HL2	HL2	HL2	HL2
1010	000	HL2	HL2	HL2	HL2



Main FUNC = TYPEC CONNECTOR

Type-C Connector

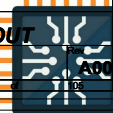


71 USB1_SSRX_CON_N1 <<<<
71 USB1_SSRX_CON_P1 <<<<
71 USB1_SSRX_CON_N2 <<<<
71 USB1_SSRX_CON_P2 <<<<
71 USB1_SSTX_CON_N1 >>>>
71 USB1_SSTX_CON_P1 >>>>
71 USB1_SSTX_CON_N2 >>>>
71 USB1_SSTX_CON_P2 >>>>

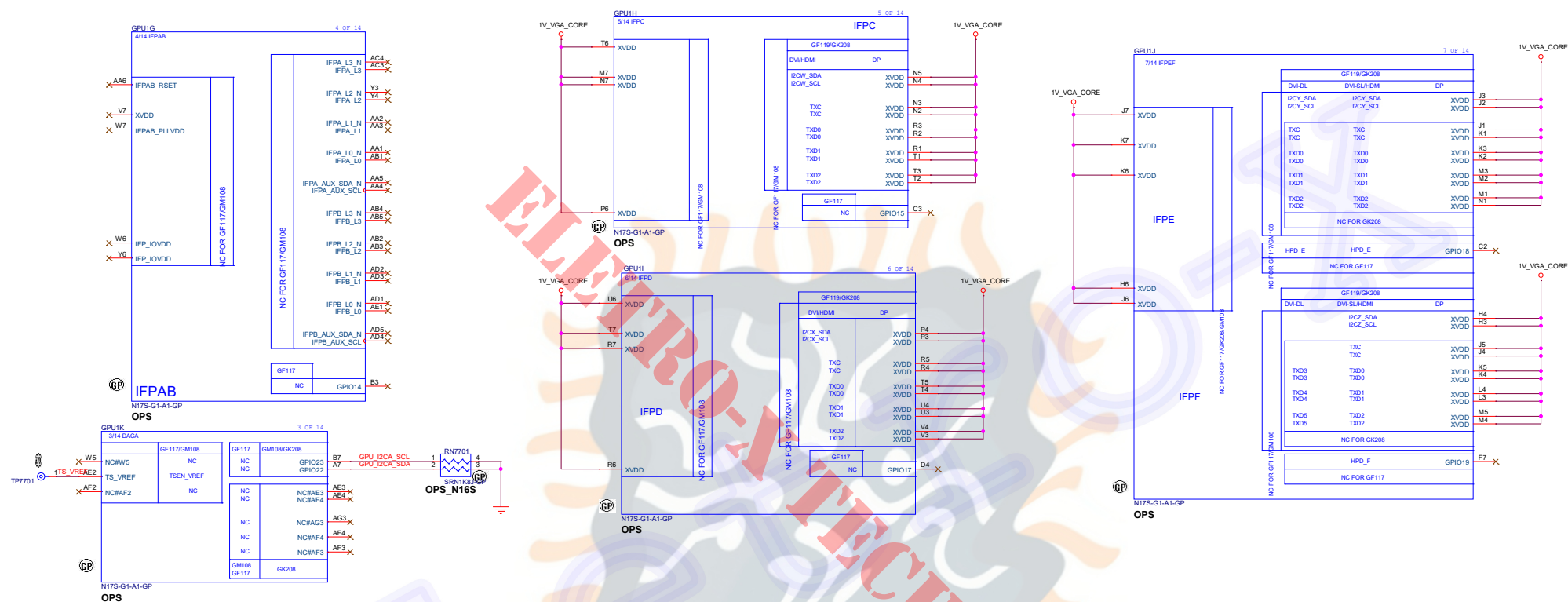
71 USB1_SBU1 >>>>
71 USB1_SBU2 >>>>
72 USBC1_CC1_CONN >>>>
72 USBC1_CC2_CONN >>>>

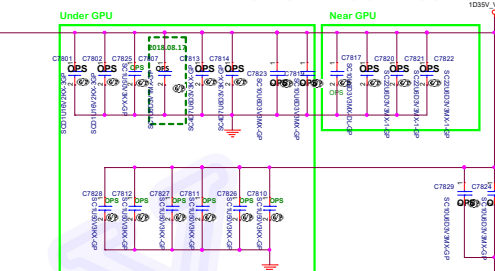
From USB2.0/ I2C Mux

71 TOP_MUX_P <<<<
71 TOP_MUX_N <<<<
71 BOT_MUX_P <<<<
71 BOT_MUX_N <<<<









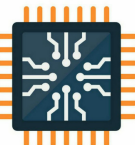
GPU Package Type	Capacitor Type		Footprint		Population	Location
GB2B-64/ GB2-64 GDDR5	0.1 μ F	X7R	0402	2	2	Under GPU
	1 μ F	X7R	0603	2	2	Under GPU
	4.7 μ F	X6S	0603	2	2	Under GPU
	10 μ F	X5R	0805	1	1	Hear GPU
	22 μ F	X5R	0805	1	1	Hear GPU



Under GPU Near GPU

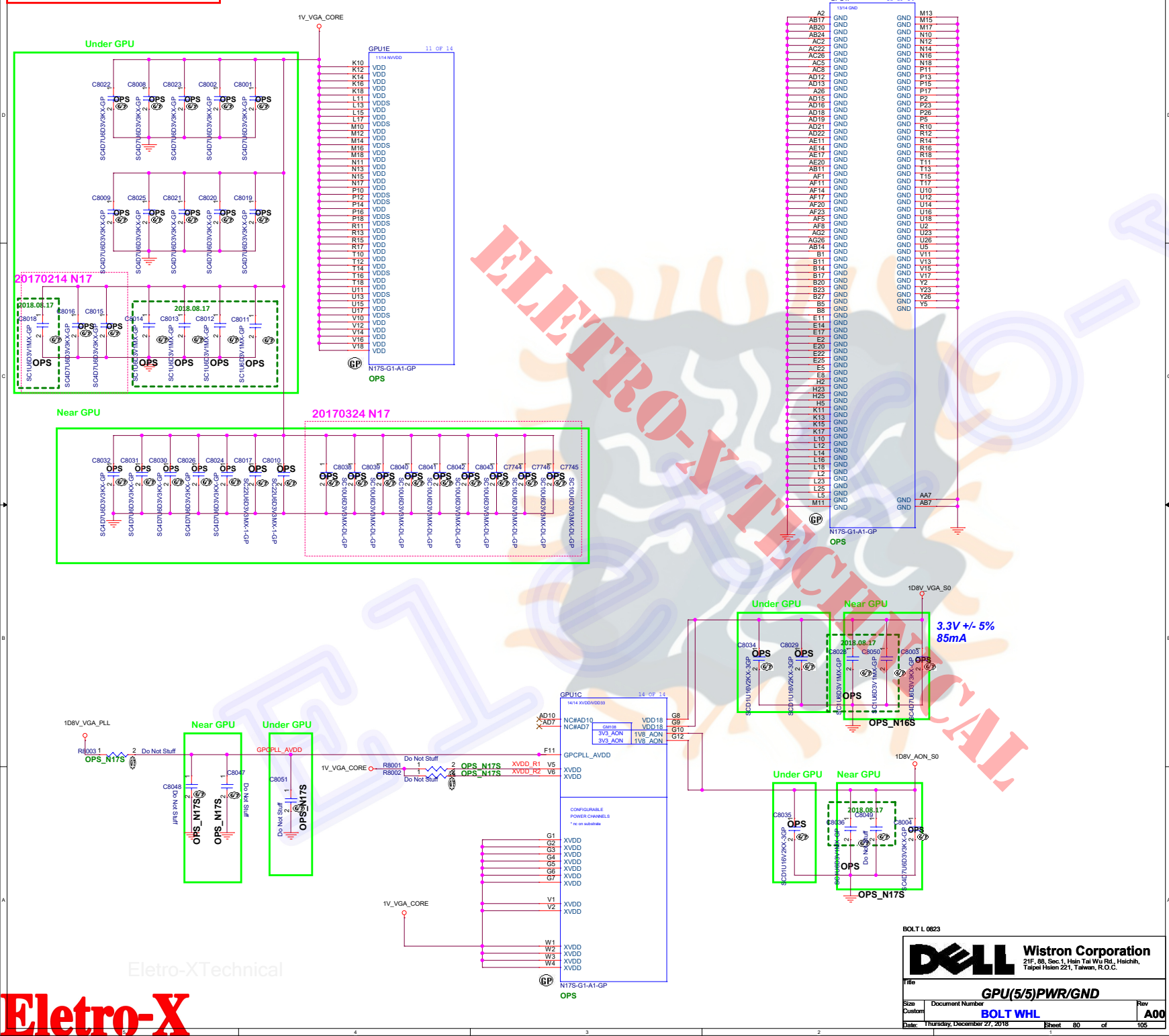


GPU Package	PLL Rails	Capacitor Type	Footprint	Population	Location	
GB38-256	GPCPLL_AVDD0/1 + LX5_PLLVDD + FB_PLL_DLL_AVDD0/1	0.1 μ F	X7R	0402	5	Under GPU
		22 μ F	X5R	0805	1	Near GPU
		Bead Type				
		30 Ω (ESR=0.010 Ω)	0603	1		Near GPU





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File		GPU(4/5)GPIO/STRAP	
Size	Document Number	BOLT WHL	
Category		A00	
Date	Thursday, December 27, 2018	Sheet	20 of 105



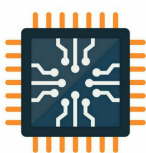
Eletro-XTechnical

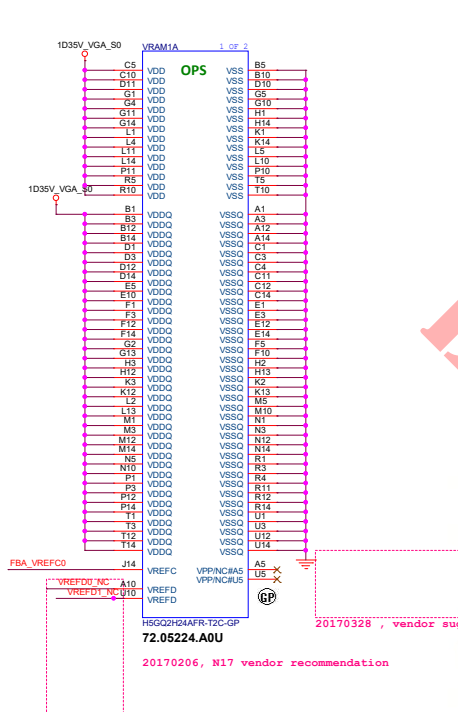
Eletro-XTechnical

Eletro-X

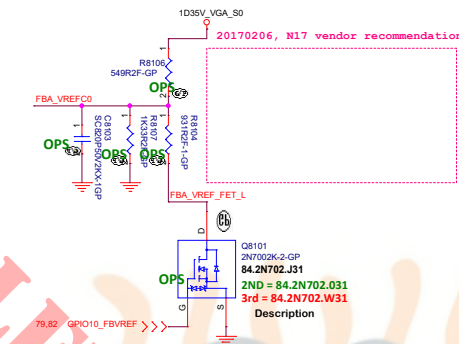
BOLT L 0823

DELL		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsein 221, Taiwan, R.O.C.			
File		GPU(5/5)PWR/GND	
Size	Document Number	Rev	
Custom	BOLT WHL	A00	
Date	Thursday, December 27, 2018	Sheet	80 of 105



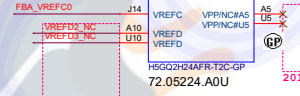
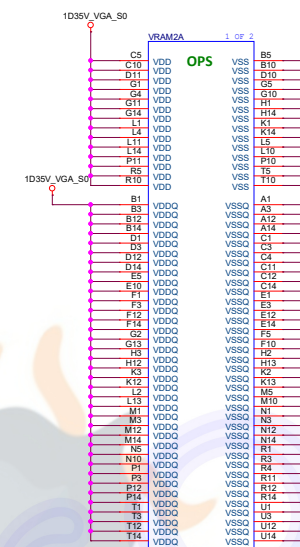


Frame Buffer Patition A-Lower Half

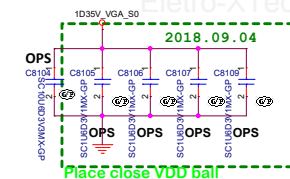


FBVREF Termination

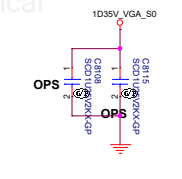
Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low



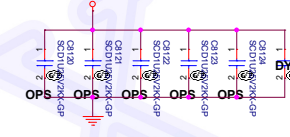
Place close VDD ball



Place close VDD ball



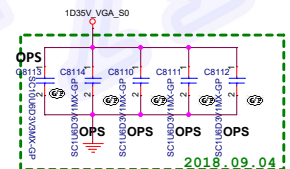
Place close VDDQ ball



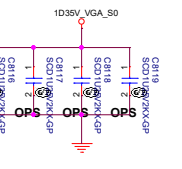
Place close VDDQ ball



Place close VDDQ ball

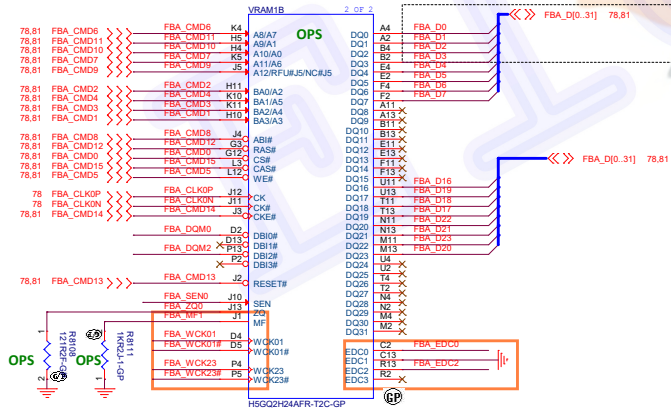


Place close VDDQ ball



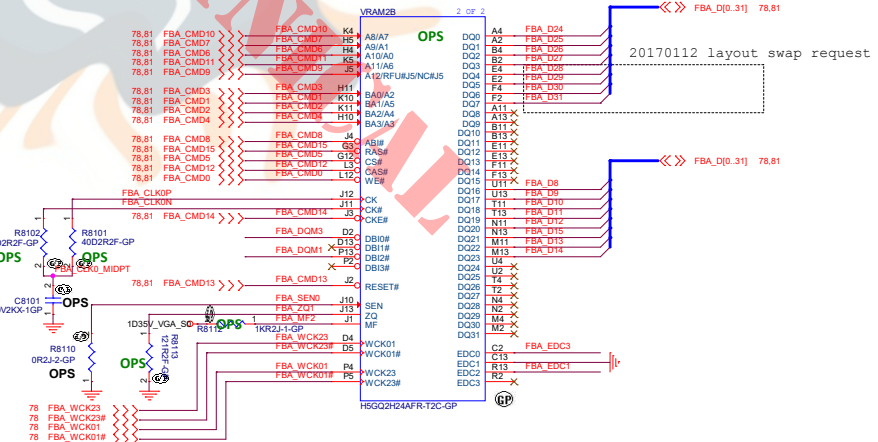
Normal(MF=0)

20170207 layout swap request



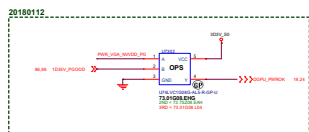
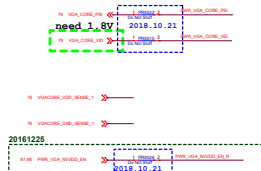
Mirrored(MF=1)

20170112 layout swap request

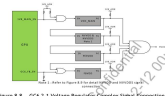


BOLT L 0823

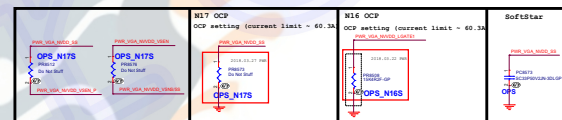
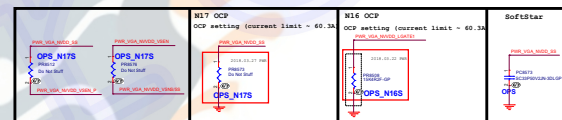
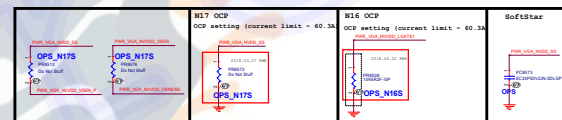
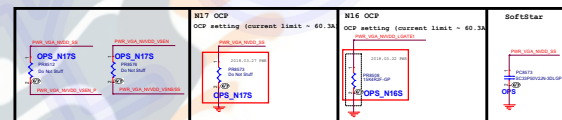
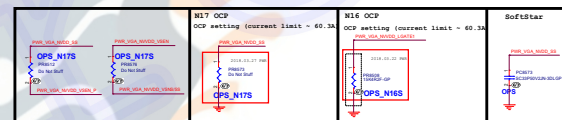
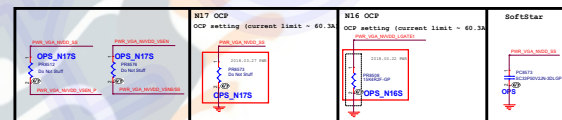
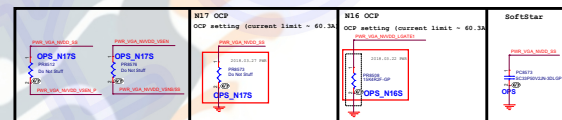
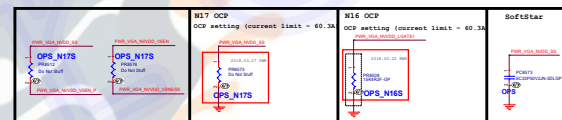
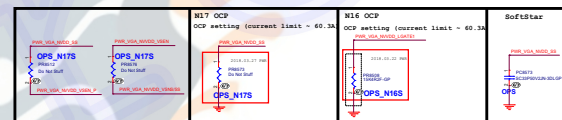
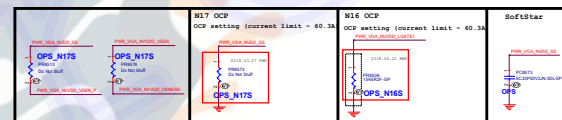
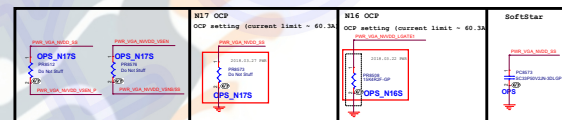
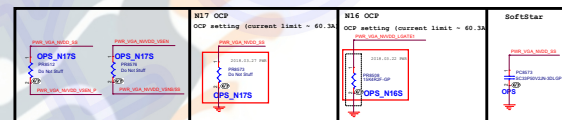
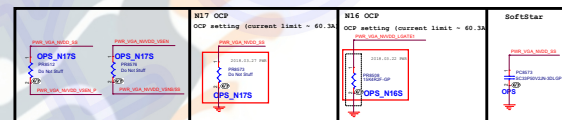
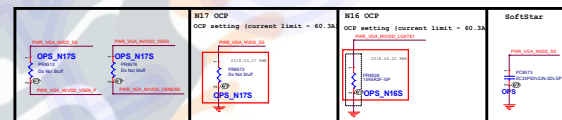
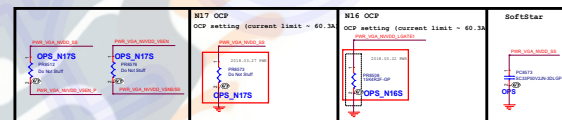
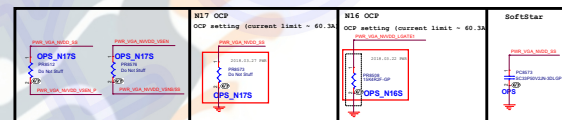
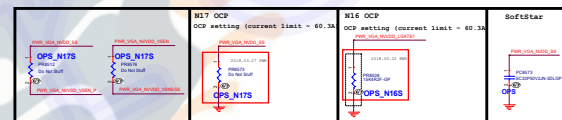
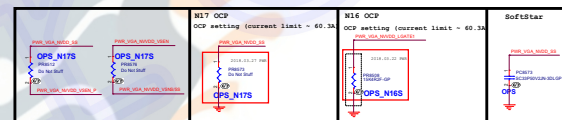
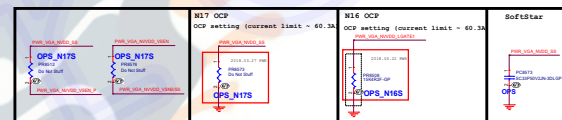
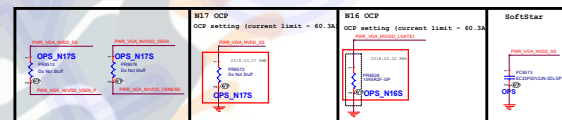
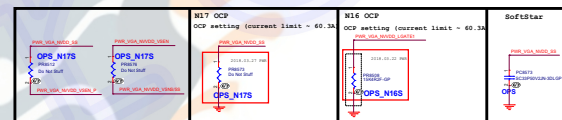
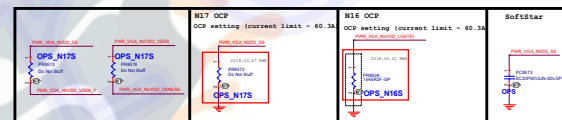
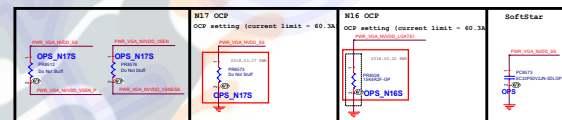
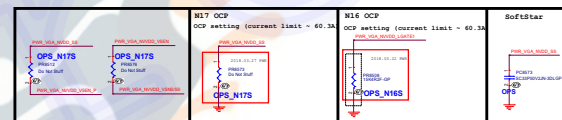
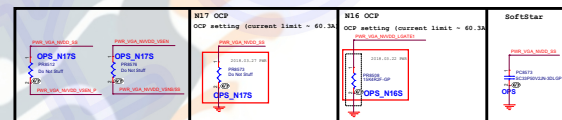
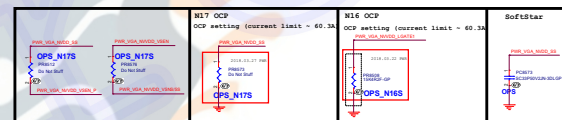
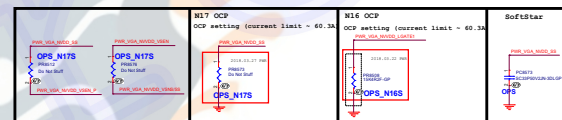
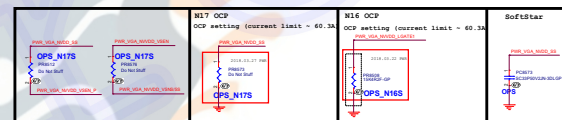
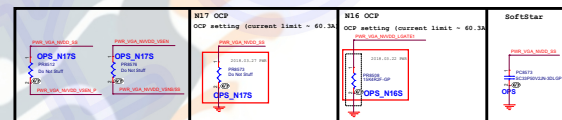
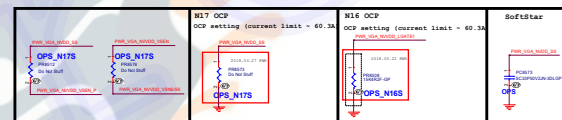
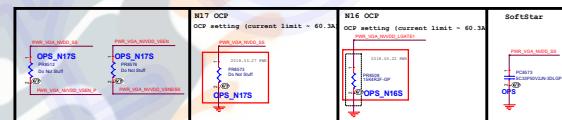
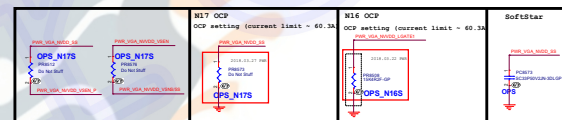
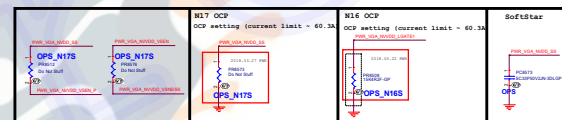
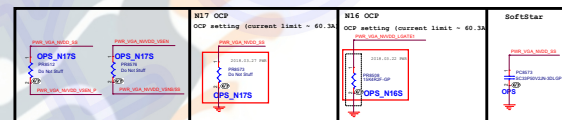
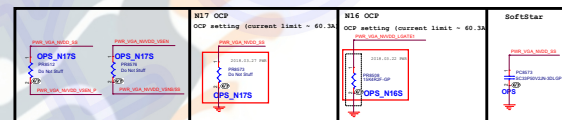
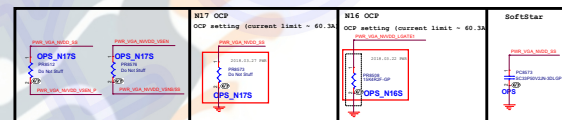
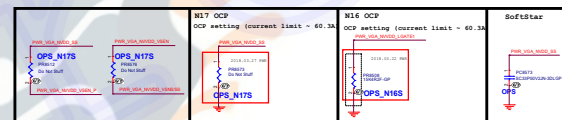
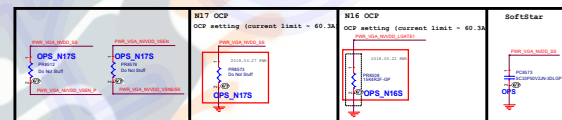
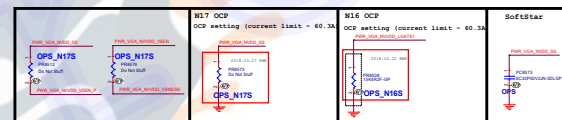
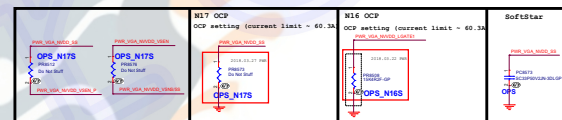
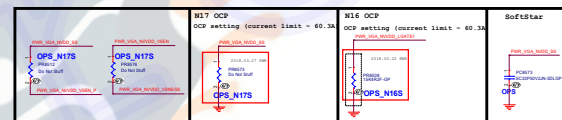
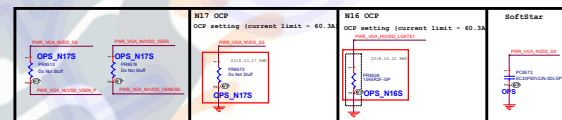
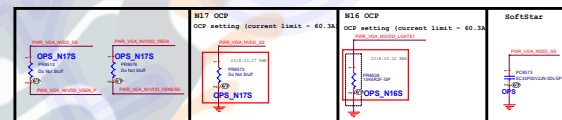
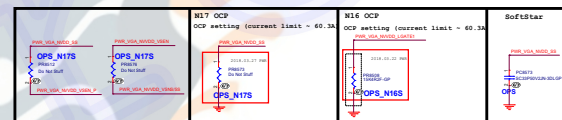
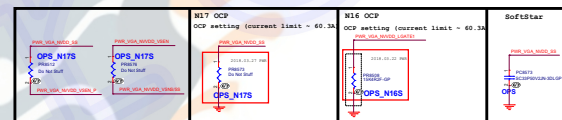
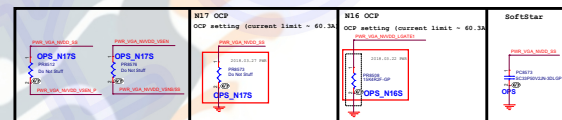
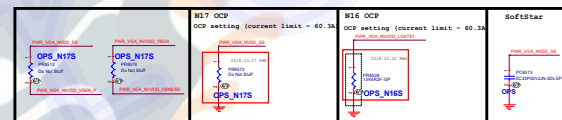
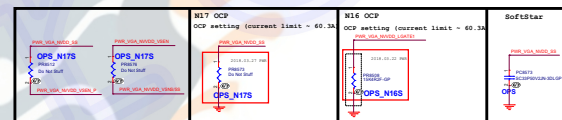
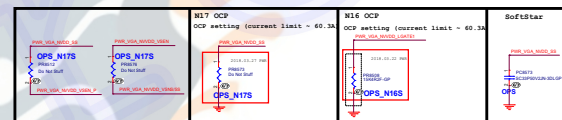
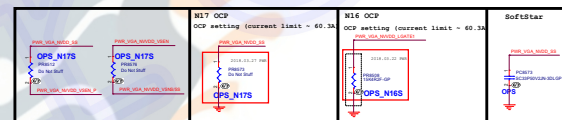
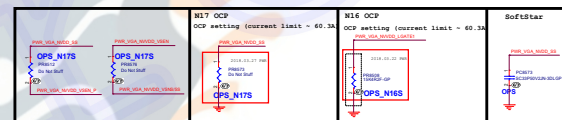
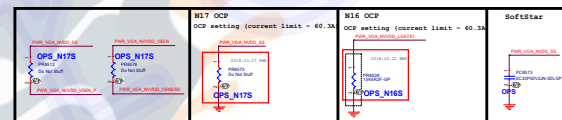
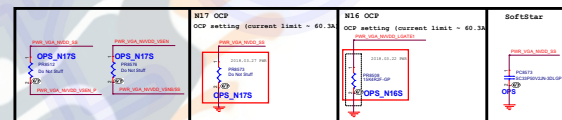
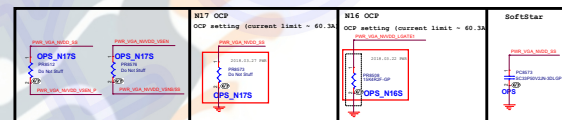
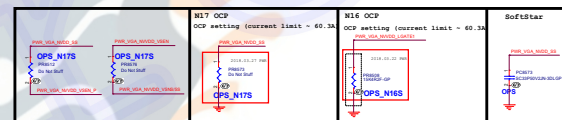
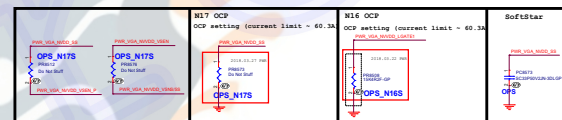
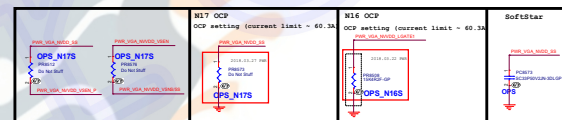
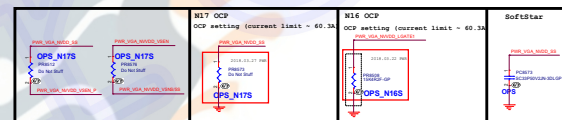
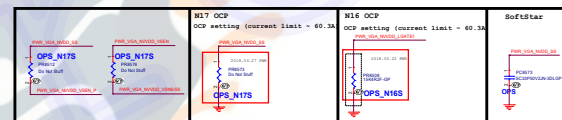
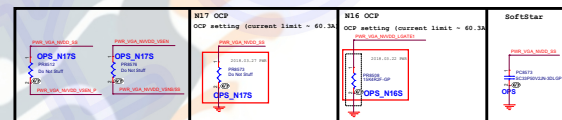
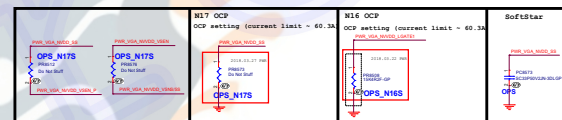
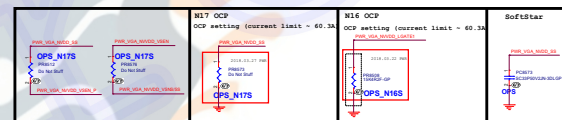
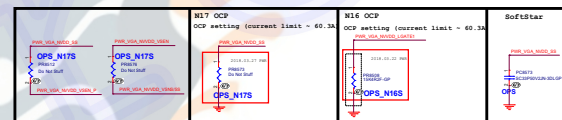
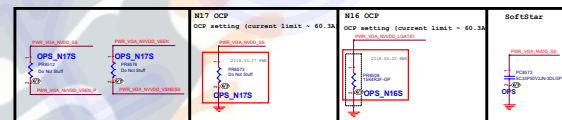
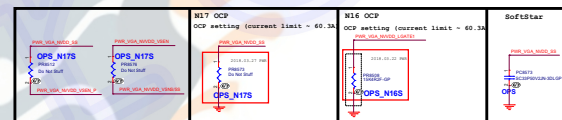
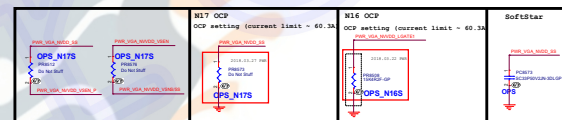
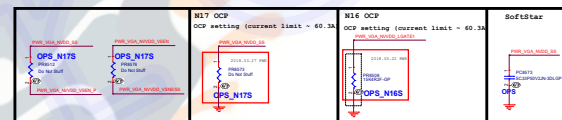
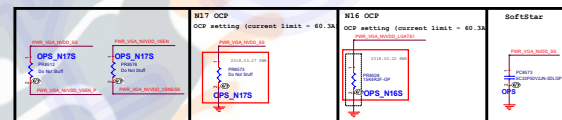
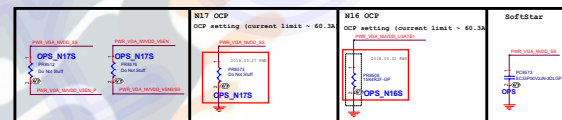
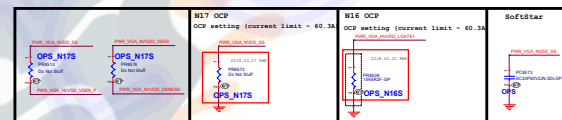
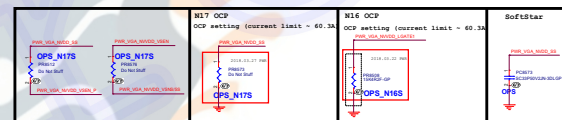
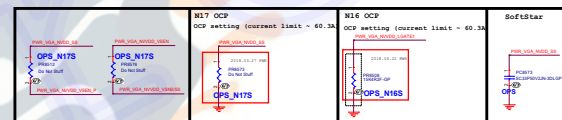
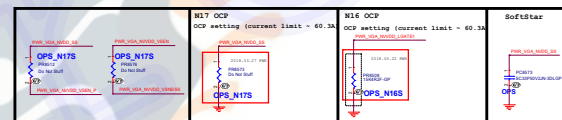
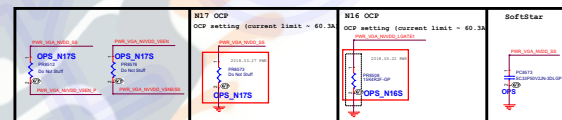
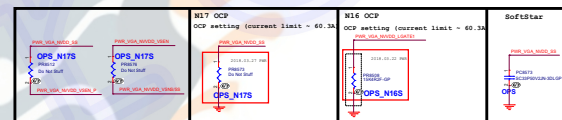
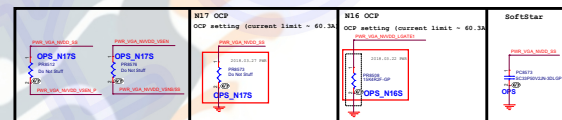
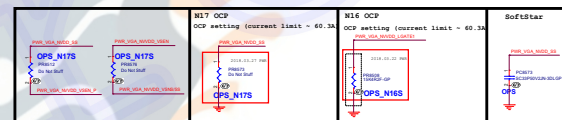
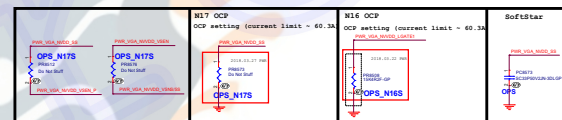
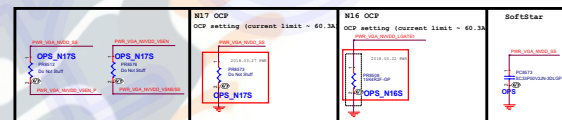
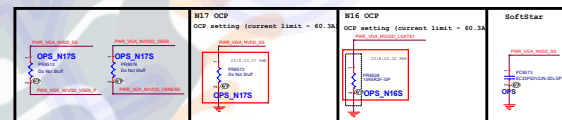
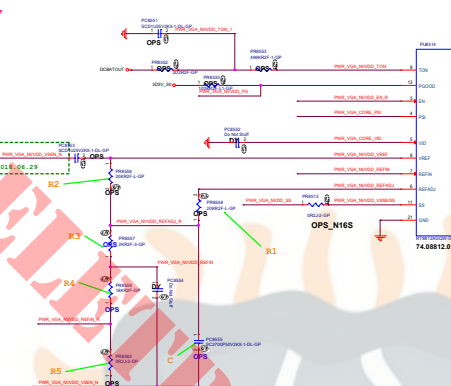
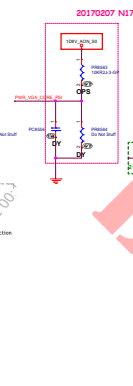
RT8812A/RT8816A For NVVDD

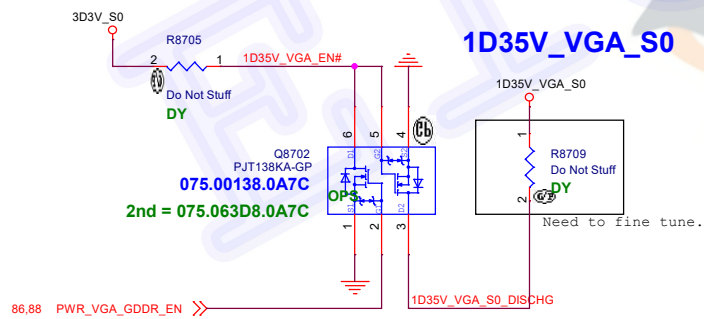
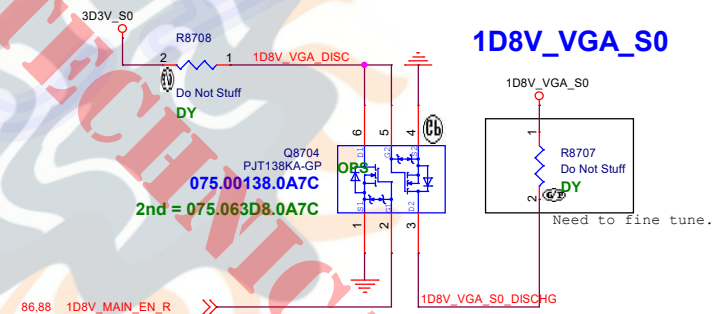
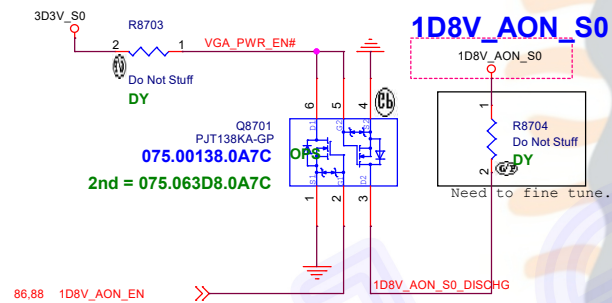
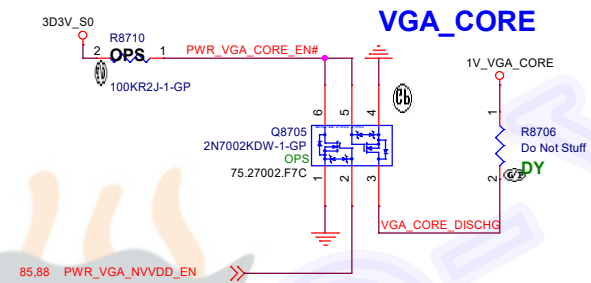
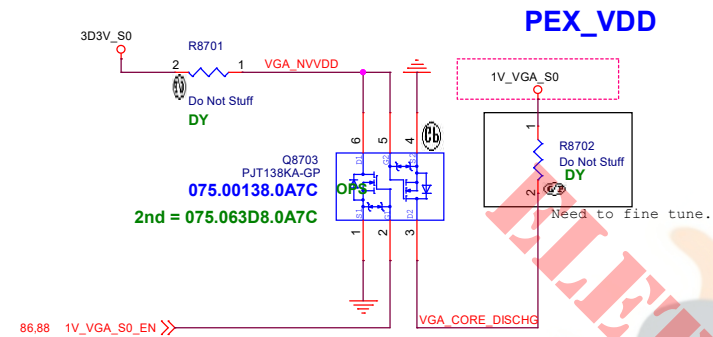


Operation Phase Number	PS1 Voltage Setting
Startup with DEM	0.7V to 0.8V
Startup with CCM	0.7V to 0.8V
Startup with DEM	1.08V to 1.35V
Startup with CCM	1.08V to 1.35V



Item	Location	N16	N17
1	RT8812A	RT8812A	RT8812A
2	RT8812A	RT8812A	RT8812A
3	RT8812A	RT8812A	RT8812A
4	RT8812A	RT8812A	RT8812A
5	RT8812A	RT8812A	RT8812A
6	RT8812A	RT8812A	RT8812A
7	RT8812A	RT8812A	RT8812A
8	RT8812A	RT8812A	RT8812A
9	RT8812A	RT8812A	RT8812A
10	RT8812A	RT8812A	RT8812A
11	RT8812A	RT8812A	RT8812A
12	RT8812A	RT8812A	RT8812A
13	RT8812A	RT8812A	RT8812A
14	RT8812A	RT8812A	RT8812A
15	RT8812A	RT8812A	RT8812A
16	RT8812A	RT8812A	RT8812A
17	RT8812A	RT8812A	RT8812A
18	RT8812A	RT8812A	RT8812A
19	RT8812A	RT8812A	RT8812A
20	RT8812A	RT8812A	RT8812A

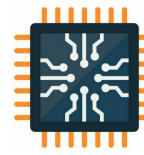
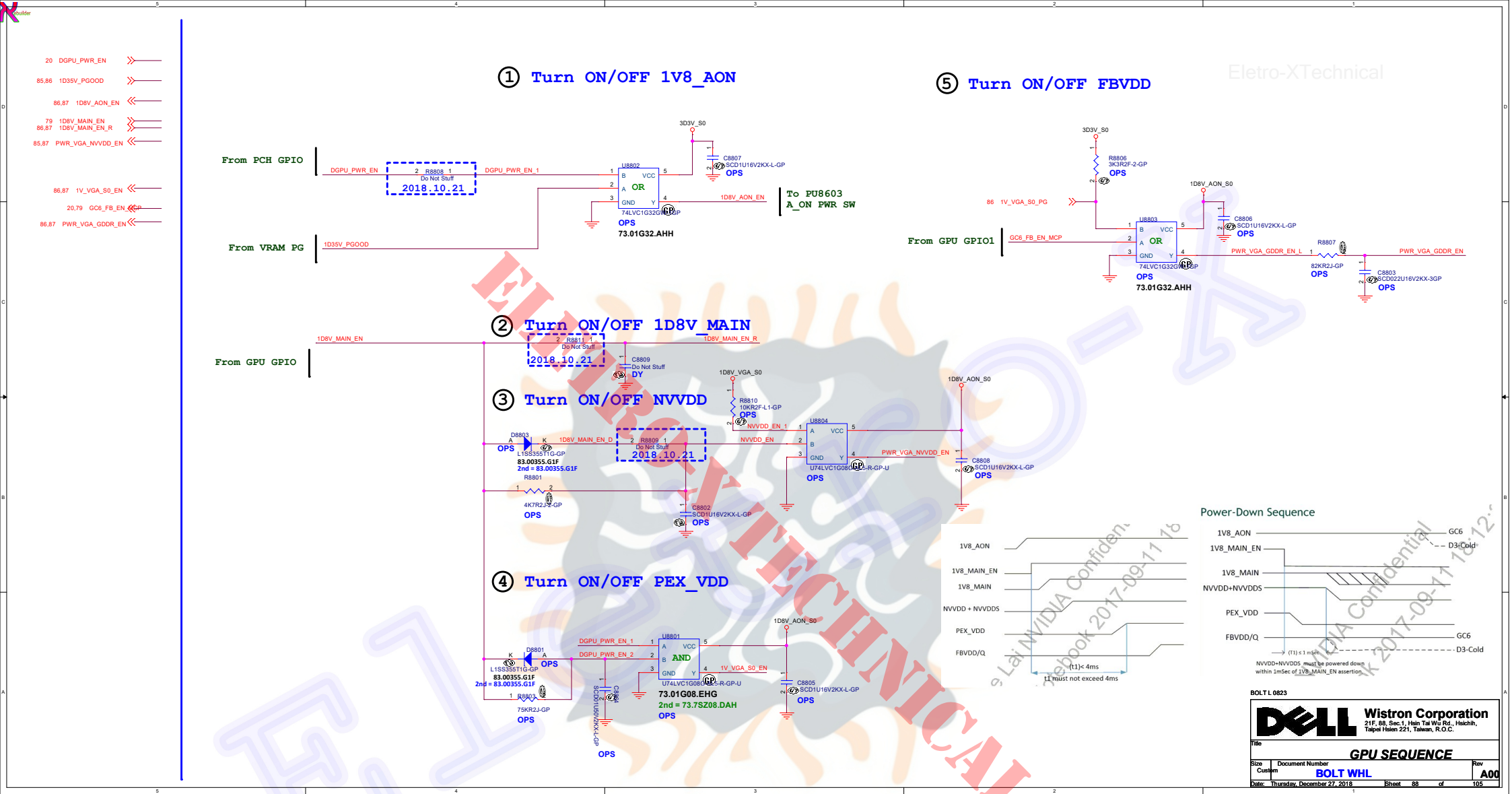




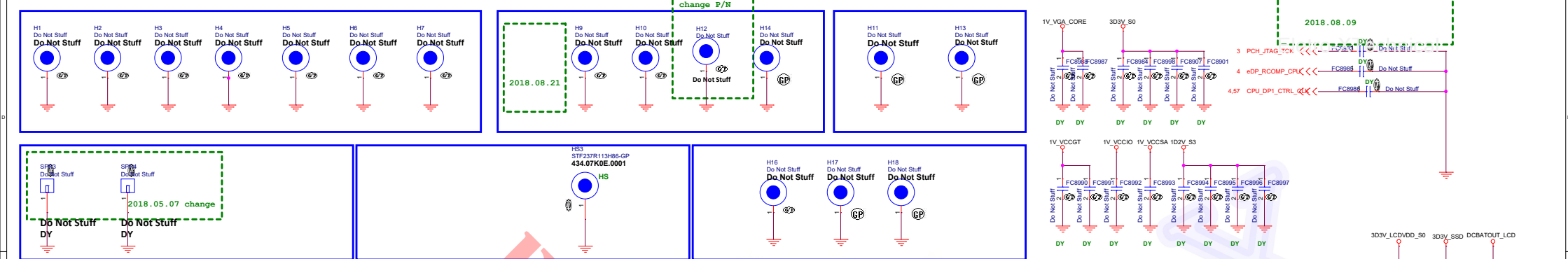
BOLT L 0823

DELL		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: Elettro-XTechnical			
Size: A3	Document Number: BOLT WHL		
Date: Thursday, December 27, 2018	Sheet: 87	of 93	

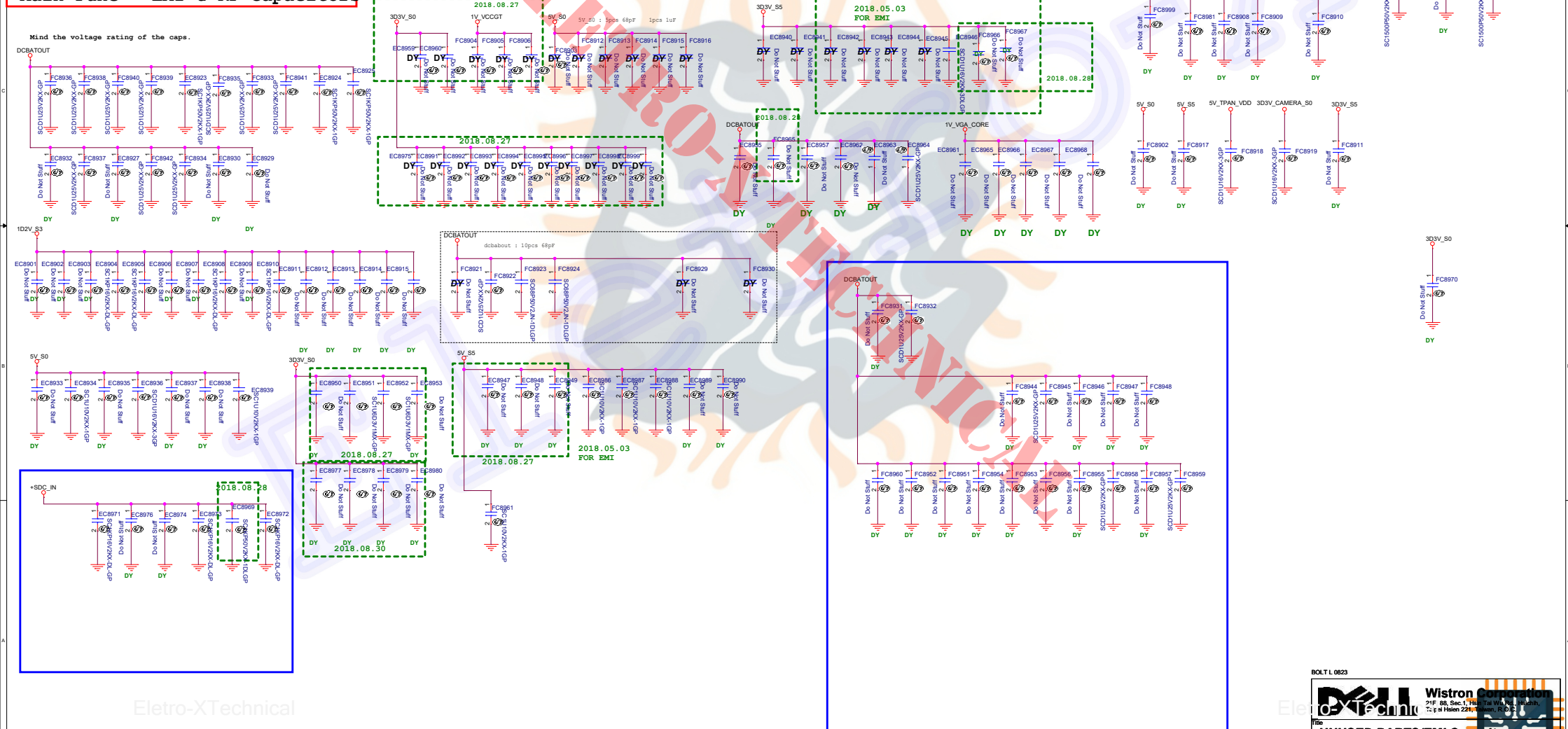




5
Main Func = UnusedParts

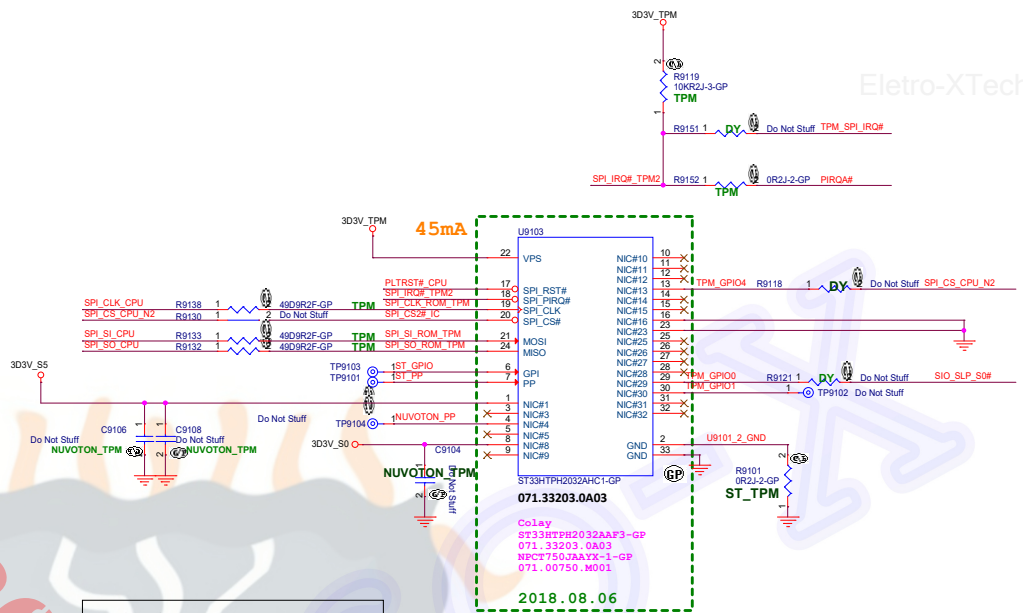
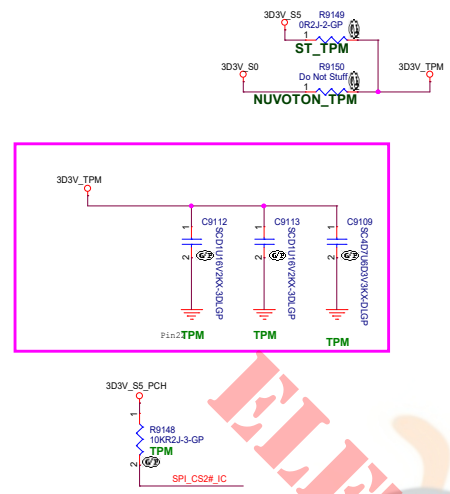


Main Func = EMI & RF Capacitors




Main Func = TPM

18,25 SPI_S0_CPU <<< _____
18,25 SPI_CLK_CPU >>> _____
15,18,25 SPI_SI_CPU >>> _____
18 SPI_CS_CPU_N2 <<< _____
17,26,31,61,62,63,76 PLTRST#_CPU >>> _____
17,40 SIO_SLP_S0# >>> _____
20 PIRQA# <<< _____
18 TPM_SPI_IRQ# <<< _____



R9133/R9132/R9138		
CPU TYPE	CNL(16M+8M)	WHL(16M)
Bolt_L(TPM)	64.33R05.6DL	64.49R95.6DL
Bolt (non TPM)	DY	DY

BOLT L 0823

**Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsein 221, Taiwan, R.O.C.

Title**TPM2.0**

Size
Custom

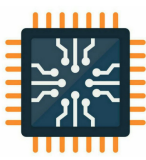
Document Number**BOLT WHL**

Date
Thursday, December 27, 2018

Rev
A00

Sheet
91

of
105

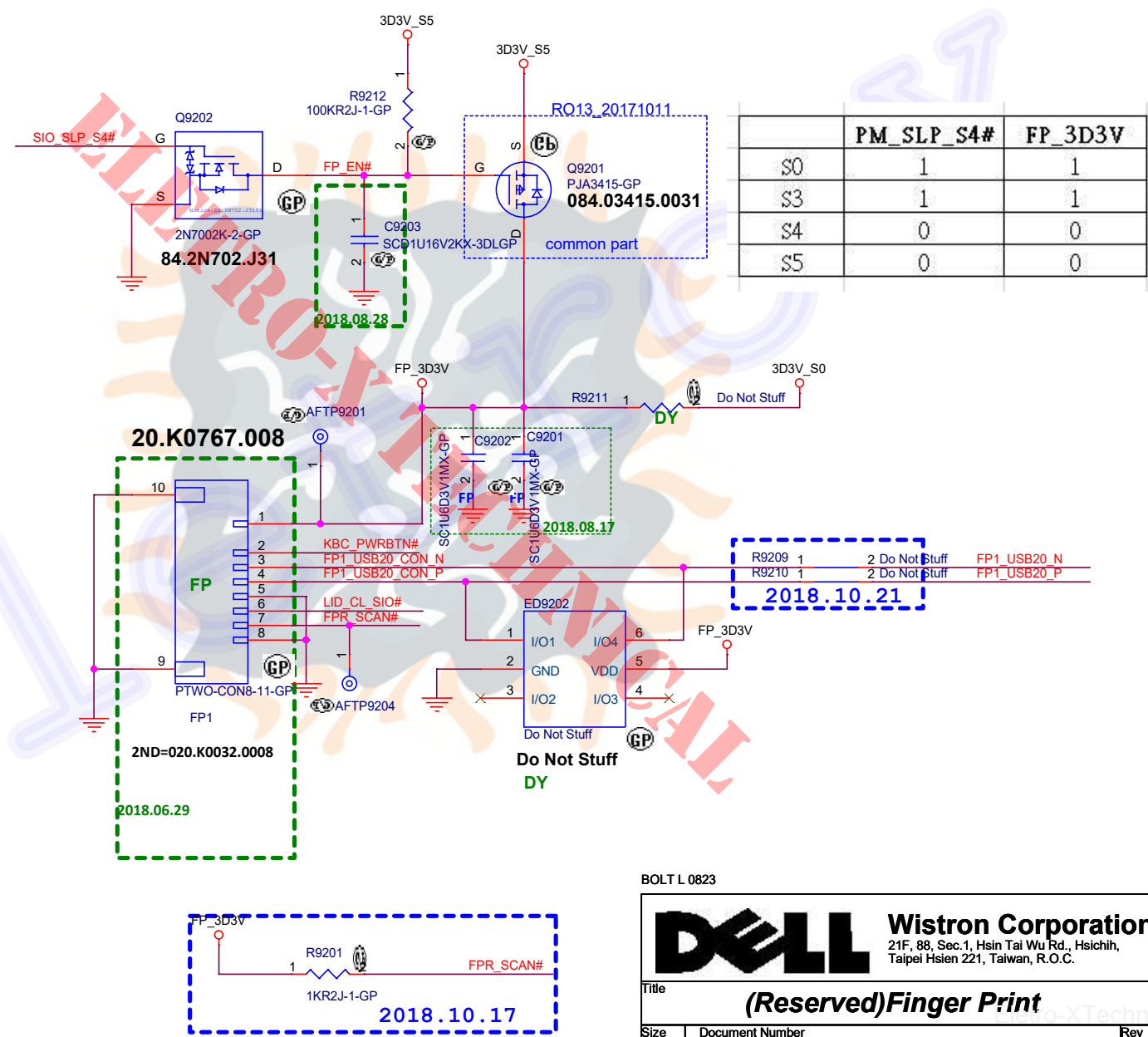


Main FUNC = FPR

Eletro-XTechnical

FBR(Botton side finger Print Sensor)

- 16 FP1_USB20_N >>>
- 16 FP1_USB20_P >>>
- 17,40,51 SIO_SLP_S4# >>>
- 24,64 KBC_PWRBTN# >>>
- 24 FPR_SCAN# >>>
- 24,64 LID_CL_SIO# <<<



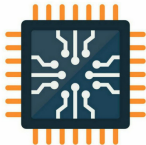
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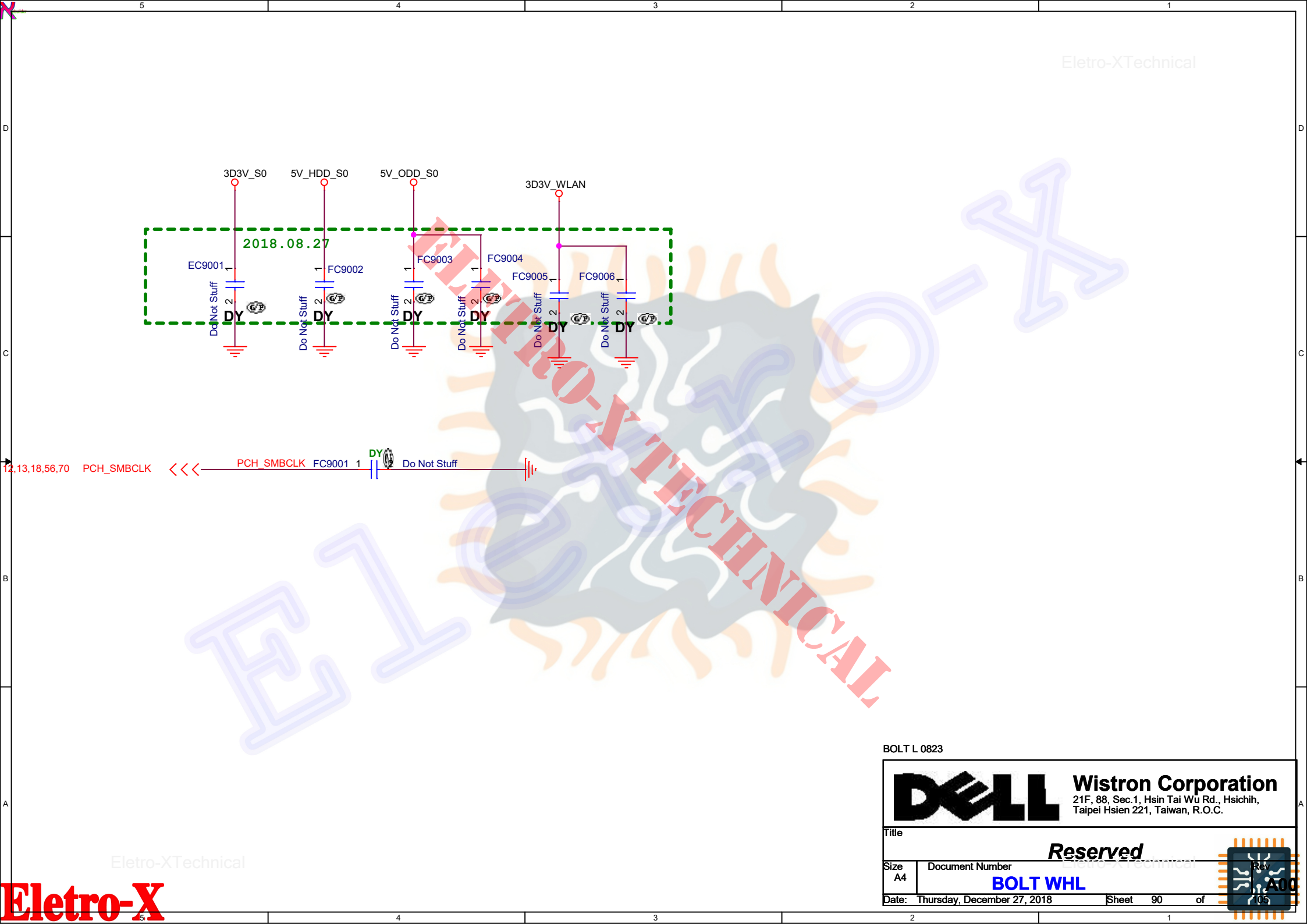
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)Finger Print


Size Custom Document Number BOLT WHL Rev A00

Date: Thursday, December 27, 2018 Sheet 92 of 106



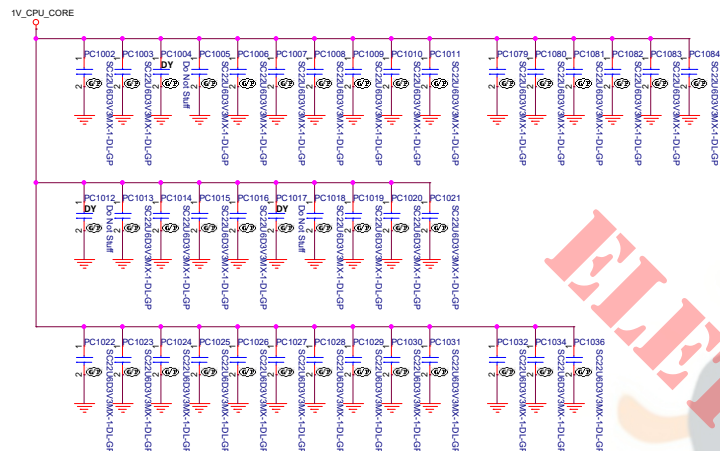


BOLT L 0823

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: Reserved			
Size: A4	Document Number: BOLT WHL		
Date: Thursday, December 27, 2018		Sheet: 90	of 105

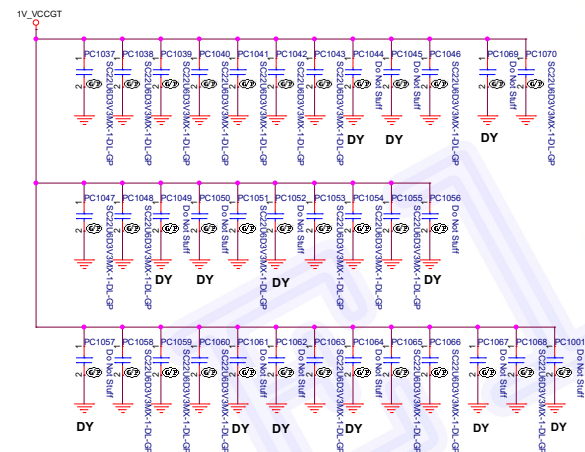
1V_CPU_CORE

22U 0603 x 39 (3DY)



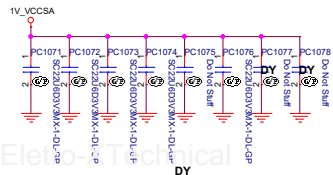
VCCGT

22U 0603 x 35 (3 DY)



VCCSA

22U 0603 x 8 (3DY)



KBL-R U42 Bulk Decoupling Example

Bulk Decoupling Locations	Example	Notes
Vcc Power Plane at VR output	2x 220 uF (@4.5mO ESR) 1x 220 uF (@4.5mO ESR)	Placed at primary side near to VR output Placed at backside side near to VR output
VCCGT Power Plane at VR output	2x 220 uF (@4.5mO ESR)	Placed at primary side near to VR output
VDDQ Power Plane at VR output	2x 47 uF 0805	Placed at primary side near to VR output
VCCIO Power Plane at VR output	2x 47 uF 0805	Placed at primary side near to VR output
VCCSA Power Plane at VR output	2x 47 uF 0805	Placed at primary side near to VR output
VCCPLL Power Plane at V1P0A VR output	1x 0.1uF 0402	Placed at primary side near to VR output

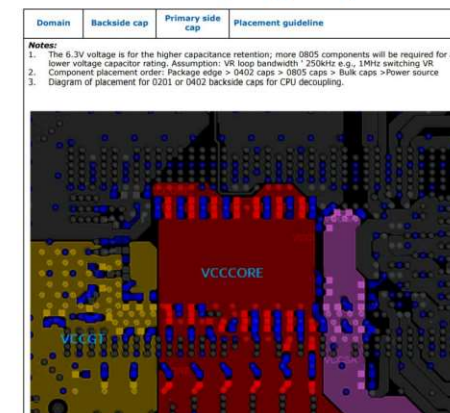
Notes:

- These examples are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.
- Bulk decoupling is not a "requirement" but recommendation only. It is an example of VR design/VR bandwidth. Customer should work with respective vendor to validate their VR & bulk decoupling designs to ensure the electrical requirements are met.

KBL-R U42 Decoupling Requirements (Sheet 1 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
Vcc	7x 10 uF 0402		Place on secondary side, underneath the package
	26x 1 uF 0402 or 0201		Refer to diagram in Note 3 below for placement recommendation of 0201 caps
		9x 22 uF 0603	Place as close to the package as possible
VCCGT	12x 10 uF 0402		Place on secondary side, underneath the package
	14x 1 uF 0402 or 0201		
		7x 22 uF 0603	Place as close to the package as possible
VCCSA	7x 10 uF 0402		Place on secondary side, underneath the package
	7x 1 uF 0402 or 0201		
		6x 10 uF 0402	Place as close to the package as possible
VCCIO		4x 1 uF 0402	Place as close to the package as possible
VDDQ		4x 10 uF 0402	Place as close to the package as possible
VDDQ		3 x 22 uF 0603	Place as close to the package as possible
VDDQ		1 x 10 uF 0402	Preferred to place the 0402 10uF cap on the secondary under the package shadow near VDDQ pin and short to VDDQ rail under with a shape. Alternatively, if the 0402 cap cannot be placed on the backside, follow the example showed in Figure 48-3. The 0402 cap to VDDQ BGA routing should not exceed 48mm (RdC). RVP design uses trace L=450mil, W=8mil between BGA and cap. Additional trace routing implemented in RVP design was not required.
VCCPLL		1x 1 uF 0402	Place as close to the package as possible.
VCCPLL_OC		1x 1 uF 0201	Do not route VCCPLL, VCCPLL_OC, VCCGT closest adjacent layer over any power net other than ground.
VCCGT		1x 1 uF 0402	For VCCGT: Refer to Figure 48-2 for additional routing details for VCCST & VCCSTG.

KBL-R U42 Decoupling Requirements (Sheet 2 of 2)



BOLT 0823

GPP_B18 / GPIO_MOSI	No Reboot	Rising edge of PCH_PWROK	<p>The signal has a weak internal pull-down. 0 = Disable "No Reboot" mode. (Default) 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running TTP/XDP.</p> <p>Notes:</p> <ol style="list-style-type: none"> 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is the primary well.
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GPP_C2 / SMBALERT#	TLS Confidentiality	Rising edge of RSMRST#	<p>This signal has a weak internal pull-down.</p> <p>0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)</p> <p>1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.</p> <p>Notes:</p> <ol style="list-style-type: none"> 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
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			<p>This signal has a weak internal pull-down.</p> <p>0 = LPC is selected (for EC). (Default)</p> <p>1 = eSPI is selected (for EC).</p> <p>Notes:</p> <ol style="list-style-type: none"> The internal pull-down is disabled after RSMRST# de-asserts. This signal is in the primary well. <p>Warning: If this strap is configured to '0' (eSPI is disabled), the eSPI Flash Sharing Mode strap must be configured to '0' as well (SAFS is disabled)</p>
GPP_CS / SMI0ALERT#	eSPI or LPC	Rising edge of RSMRST#	



SPD0_MOST	Reserved	Rising edge of RSMRST#	<p>External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.</p> <p>This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.</p>
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GPP_D12 / ISH_SPI_MOSI / GSP12_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HGM. There should NOT be any on-board device driving it to opposite direction during strap sampling.
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SP10_102	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
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SPIO_I03	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
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HDA_SDO / 1250_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWROK	<p>This signal has a weak internal pull-down.</p> <p>0 = Enable security measures defined in the Flash Descriptor. (Default)</p> <p>1 = Disable Flash Descriptor Security (<i>override</i>). The strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY.</p> <p>Notes:</p> <ul style="list-style-type: none"> 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
-----------------------	---	-----------------------------	--



GPP_H21	XTAL Frequency Select	Rising edge of RSMRST#	<p>This signal has a weak internal pull-down. An external pull-up is required on this strap since 3 MHz XTAL is not supported on the PCH.</p> <p>0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected.</p> <p>Notes:</p> <ol style="list-style-type: none"> 1. The internal pull-down is disabled after RSMRST de-asserts. 2. This signal is in the primary well.
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GPP_F6 / CNV_RGI_DT	M.2 CNV Mode Select	Rising edge of RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVI enable. 1 = Integrated CNVI disable.
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INPUT3VSEL	3.0V Select	<p>Input pin must always be driven to a valid logic level</p> <p>External pull-up or pull-down is required 0 = 3.3V supply is 3.3V +/- 5% 1 = 3.3V supply is 3.0V +/- 5%</p> <p>Note: This strap should only be used for specific targeted 1S battery systems.</p>
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GPDP7	Reserved	Rising edge of DSW_PNROK This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling	External pull-up is required. Recommend 100K.
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GPP_H23	eSPI Flash Sharing Mode	Rising edge of RSMRST#	<p>This signal has a weak internal pull-down.</p> <p>0 = Master Attached Flash Sharing (MAFS) enabled (Default)</p> <p>1 = Slave Attached Flash Sharing (SAFS) enabled.</p> <p>Notes:</p> <ul style="list-style-type: none"> 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. <p>Warning: This strap must be configured to '0' (SAFS is disabled) if the eSPI or LPC strap is configured to '0' (eSPI is disabled).</p>
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[ROM Only] PHYSICAL_DEBUG_ENABLED (DPP PRIVACY)	
0	DISABLED
1	INT DPP SHARED BIT IN DEBUG INTERFACE HUB
2	DISABLED



(R4301A)
 SINGAPORE PORT FIRMWARE STRAP
 (R4301A)
 No Physical Singing Port attached to Embedded SingingPort'. No connect for dislink.



Eleetro-XTechnical

